White Paper

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Testing Low Power Designs with Power-Aware Test

Manage Manufacturing Test Power Issues with DFTMAX™ and TetraMAX®

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Introduction

The most important trend over the past decade for semiconductor design is the dominant requirement to reduce power consumption and power dissipation. Not only do competitive products require more functionality and higher performance, they must fit into increasingly smaller and more portable products. Because battery technology has only experienced marginal improvements over this same period of time, designers must consider a wide variety of new circuit techniques to reduce power beyond the traditional scaling provided by Moore's Law.

Design teams must also address the broad impact of low power design techniques on design-for-test (DFT) and on manufacturing test. This white paper describes five key areas that must be considered for comprehensive testing of low power designs, and the automation provided by DFTMAX and TetraMAX to manage each of these new challenges:

- Optimized DFT for low power designs
- Reducing DFT power in mission mode
- Higher test quality with power-aware ATPG
- Testing power management circuitry
- Verifying test on low power designs

Optimized DFT for Low Power Designs

Almost all low power designs use techniques that require special awareness and optimizations in the DFT architecture and the process of synthesizing DFT logic. Multiple voltage domains require dedicated level shifter cells for all signal crossings between voltage domains, and scan chains are no exception. Thus, the scan chain architecture should not only reduce area overhead and routing congestion, it should also reduce or eliminate individual scan chain crossings between voltage domains. Grouping and ordering scan chains without awareness of voltage domains could result in a huge increase in the number of level shifters required, which would create unnecessary area overhead and circuit delays.

Another common technique is power gating, whereby specific functional units of a device can be individually powered down when their operation is not required. Isolation cells are required for all signal crossings between power gating domains, and likewise, DFT should introduce minimal signal crossings between power domains. If the device will ever be tested with one or more power domain in an inactive state, it is critical that scan chains in any active power domain operate independently from those in any inactive power domain. Besides the scan chains, scan compression logic must consider power domains. Each compressor-decompressor (CODEC) module should be in the same power domain as the connected scan chains to minimize isolation cells, and each power domain may require a separate CODEC to maintain testing independence between power domains. Figure 1 shows a graphical example of optimal chains and scan compression in a typical low power design.

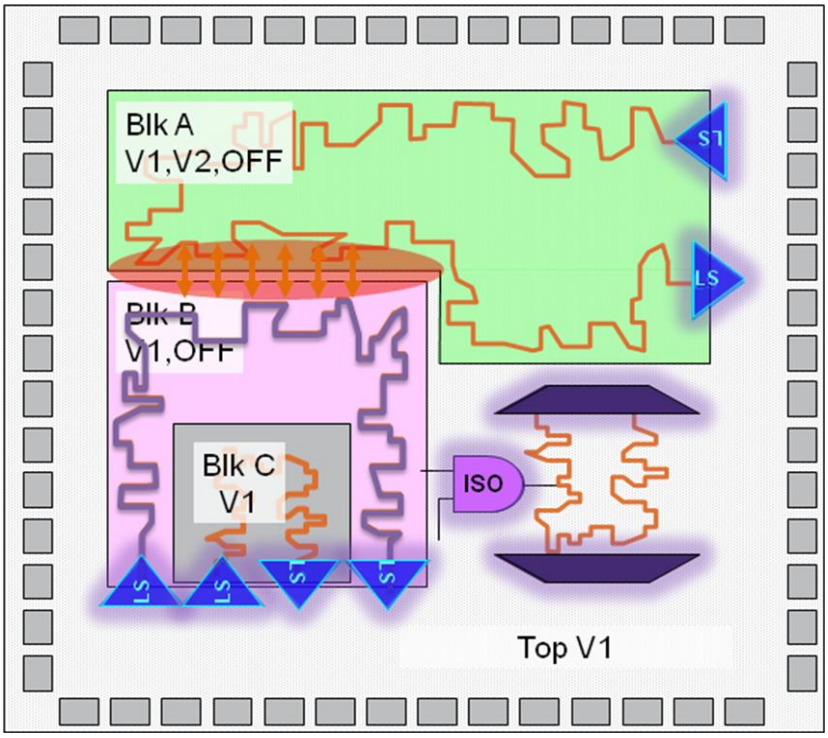

Figure 1: Optimized DFT in a low power design

Finally, retention cells may introduce special DFT requirements. Most importantly, synthesis must properly insert and connect complex sequential cells which incorporate both retention and scan functionality. Depending on the retention cell design and testing methodology, retention states may be connected along separate, dedicated scan chains which can be shifted even when the normal functional state is powered down.

DFTMAX optimizes DFT for low power designs with minimal additional user intervention. The same IEEE 1801 specification (also referred to as UPF) for logic synthesis is also used by DFT synthesis. Since DFTMAX operates completely within the Design Compiler environment, there is a single, common interpretation of the UPF specification.

Reducing DFT Power in Mission Mode

In addition to optimizing DFT in low power designs, it is also important that any DFT circuitry not increase the dynamic power consumption when the device is running in its mission mode - i.e., in the functional state. There are several ways in which DFT may inadvertently increase power other than during test mode. The first is switching activity on dedicated scan chain nets. Some libraries contain scan cells with a dedicated scan output pin, usually a buffered version of the functional output. Synthesis must properly support scan cells which also gate this dedicated scan output during functional mode to minimize switching activity on separate scan chain nets.

The second source of unnecessary power consumption is from spurious switching activity created within the compression logic. DFTMAX uses combination compression, which is logically constructed of XOR trees. The inputs to these XOR trees are the outputs of all the internal scan chains. For high levels of compression, this means many thousands of XOR gates could toggle anytime switching activity occurs within functional logic connected to that compressor. To avoid this, DFTMAX adds blocking logic to suppress all switching activity from the functional logic at the compressor inputs, except when scan chains are shifting.

Higher Test Quality with Power-Aware ATPG

Manufacturing tests for wafer sort and final package screening should test the device under the full range of conditions specified for its functional application. Typically these variables have been limited to voltage, temperature, and clocking frequencies. But the characteristics of internal switching activity can have a substantial impact on the quality of a test program. Let's consider two scenarios. In the first, the switching activity generated by test patterns is double that ever encountered during functional mode. Since the power rails in the device are designed for functional operation, this increased level of switching activity will cause additional and potentially excessive IR drop. This effect will be most pronounced in the center of the die, and the lower voltage will artificially increase circuit delays; in the worst case, this will create power supply droops or glitches that may cause sequential cells to flip logic state. The end result would be that an otherwise good device will fail the test program. This type of over-testing will cause unnecessary yield loss for the product.

In the second scenario, the switching activity generated by test patterns is only half that of the functional mode. While this eliminates the chance of too much IR drop, circuits may now operate faster on the tester than they would in the actual system. For speed related and high resistance defect mechanisms, this type of under-testing means that the device would only be rejected by the systems integrator - or worse, by the end consumer. Such behavior is another source of test escapes, and will increase the DPPM (defective parts per million) metric of test quality for the device.

TetraMAX ATPG employs specialized algorithms to manage the switching activity caused by the test patterns it generates. It is necessary to consider the switching activity from two different components of a scan test pattern: shifting and capturing. For scan shifting, it is important to reduce the average switching activity across all the cycles used to shift scan states into and out of the device. The average switching activity is correlated with the average power dissipation of the device on the tester. By reducing the average shift switching activity, it is possible to shift at a greater frequency for a given junction temperature, and thus reduce the total time for scan testing and the capital cost of ATE equipment required. Figure 2 shows the switching activity across a complete pattern set generated by TetraMAX ATPG. The red points represent the shift switching activity for each ATPG pattern using only the traditional "adjacent fill" technique. The profile is very uneven - very high power dissipation and the beginning of the test pattern set, and then decreasing to much lower levels by the end of the pattern set. The light blue points indicate the shift switching activity with additional ATPG "effort" to manage the number of scan cells that will transition during each shift vector. The maximum power has been reduced by 2X, and the profile is much more even.

If shift power needs to be reduced by a further amount, DFTMAX also supports the automatic insertion of gating logic on the functional outputs of scan cells. By blocking the functional data path during scan shift, combinational logic remains stable when shifting scan chains. This technique can increase circuit area, but power-aware optimizations are employed to gate only those scan cells with the largest contribution to functional logic switching activity.

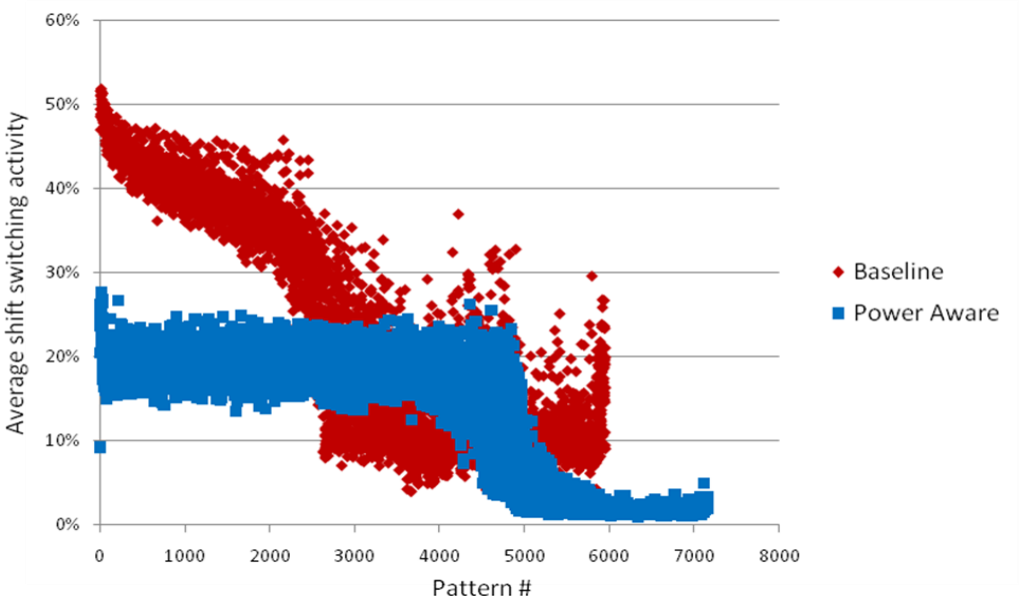

Figure 2: Shift power reduction

For capture of test responses, especially for accurate detection of delay defects, it is critical to ensure that the peak switching activity generated by both clock pulses of an at-speed test is as close as possible to the nominal functional switching activity levels specified for the device. Figure 3 shows the switching activity for each capture clock of another pattern set from TetraMAX ATPG. The three different data sets represent: a.) unconstrained switching activity (red points), b.) budget similar to functional mode (light blue points), and c.) budget below functional mode (dark blue points). Notice that the total number of patterns does not increase significantly as long as the switching budget remains at or above functional mode. If the budget is set too far below functional mode, ATPG must generate less efficient patterns and the total pattern count increases.

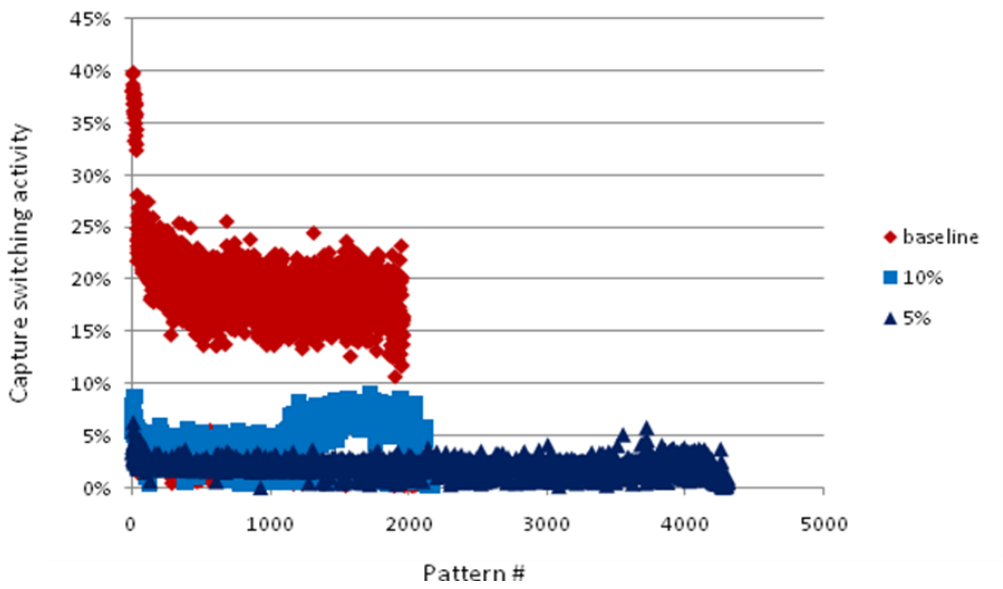

Figure 3: Capture power budget

Testing Power Management Circuitry

For designs in which all power domains are always on, the fault models supported by TetraMAX ATPG will provide high test coverage of defects on level shifters. However, for designs with powered-down states and possibly retention cells, it is necessary to test the device in multiple power states to achieve high test coverage of low power design elements; this is because there are specific defects that may not be covered by always-on testing.

DFTMAX and TetraMAX support a complete flow for this testing approach, referred to as testing by power domains. Testing a sufficient number of power states in which each switchable power domain is set to its inactive state at least once will allow these additional defects to be sensitized. Multiple techniques are then used to observe defects unique to each of the following low power design elements:

- Isolation cells – stuck-at tests for the active power domains will detect that a faulty isolation value is being driven from inactive power domains.
- Retention cells – a test sequence loads values into scan chains and pulses the sleep signal before power domains are set to an inactive state. Any incorrectly retained values will be captured back into the scan chain when the power domain is returned to its active state and the restore signal is pulsed.
- Power management – observe test points are added on the power control and acknowledge signals so that a faulty value driven from the power state logic can be directly captured in dedicated scan cells.
- Power switches – IDDQ testing will measure excessive levels of leakage current if any power switches are not fully turned off.

Verifying Test on Low Power Designs

The previous sections describe optimal DFT and test patterns for low power designs. But it is also important to perform specific design and simulation checks to verify these as well. Low power verification with MVRC, and running VCS with MVSIM provide comprehensive, robust validation of the DFT structures and power-aware test patterns. Here are some of the most important checks performed by these tools:

- Have level shifters and isolation cells been properly inserted on scan chains, test signals and in scan compression logic?
- Has DFT been properly inserted in and around the power management circuitry?
- Does the test program properly initialize the power state of the device for testing? Are power domains and power signals stable during the each scan test?

Within the overall flow, MVRC performs static checks after DFT implementation, and MVSIM validates correct power behavior during Verilog simulation of TetraMAX-generated test patterns.

Summary

The test challenges for low power designs have increased in many dimensions. In response, new DFT optimizations, ATPG algorithms, testing techniques, and verification methods have been developed within DFTMAX and TetraMAX. These capabilities are fully integrated in the complete Synopsys synthesis and test flows for maximum ease of use and minimal risk of adoption. These power-aware technologies also ensure the highest test quality and the fastest time to volume production that designers and test engineers have come to expect from Synopsys.

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