SYNOPSYS®

DATASHEET

Synopsys Totem and Totem-SC

Analog Mixed-Signal Power Integrity and Reliability Signoff

Overview

Synopsys Totem™ is a transistor-level power integrity and reliability analysis platform that enables you to perform comprehensive analysis on analog mixed-signal IP and full-custom designs. Totem redefines the traditional analog mixed-signal power noise and reliability analysis flow with support for multiple design environments for modeling and characterization. Totem features a high-capacity extraction and simulation engine along with a powerful graphical interface for root-causing and debugging analysis results.

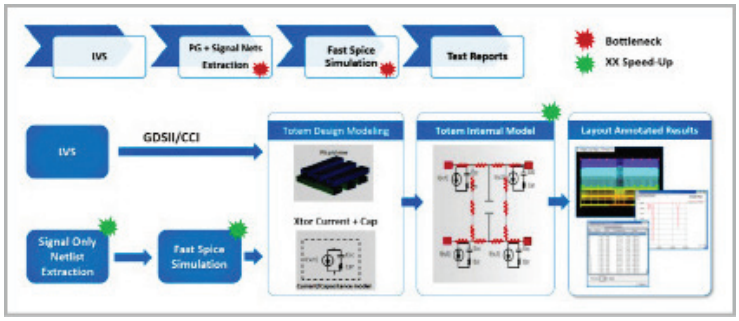

Figure 1: Totem Analog and Mixed Signal Signoff Analysis Flows

Silicon-Proven Power Integrity and Reliability

Totem, the first analog, mixed-signal power integrity and reliability simulation solution, has enabled hundreds of successful silicon implementations. In addition to static and dynamic voltage drop analyses, Totem offers other advanced analyses, such as thermal aware electromigration (EM) analysis, Electrostatic Discharge (ESD) integrity analysis, logic library EM validation, and Power Management Integrated Circuit (PMIC) analysis for analog, mixed signal, and PMIC design signoff. Totem can also include the substrate network to perform noise injection analysis, and include package and board models, for chip-package-system co-analysis.

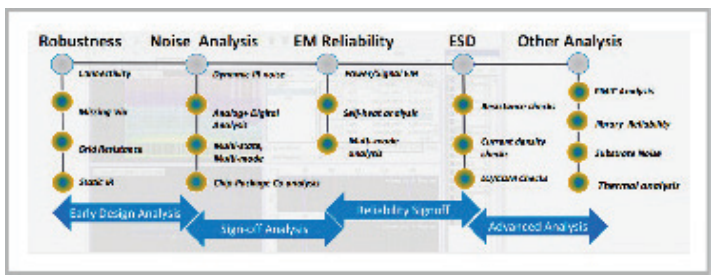

Figure 2: Totem Analog and Mixed Signal Full-Chip Analysis Coverage

Accuracy and Foundry Signoff Certification

Totem offers accurate topology and current direction-aware extraction along with a high-capacity picosecond resolution transient solver for SPICE-accurate results. Totem results correlate very well with silicon measurements, as validated by many customers, including analog and mixed signal IP vendors. Major foundry certifications for power integrity and reliability down to 3nm technology are further validation of Totem's accuracy. In addition, Totem offers a comprehensive macro modeling capability for IPs for best integration and accurate analysis at the SoC (System on Chip) level using Synopsys RedHawk-SC™.

Capacity, Performance and Advanced Debug

Multi-CPU architecture and advanced solvers enable flat simulation of 100+ million transistor designs. Totem can perform hierarchical modeling and simulation using a macro modeling approach. It also offers a rich, analysis-driven graphical user interface with several advanced debug and query capabilities that enable designers to determine the root-causes of design weaknesses. With its incremental extraction and analysis capabilities, designers can verify a fix before changing the original layout.

Early Analysis to Signoff

Totem can be used from early stages of the design to final signoff. During the early design stages, layout designers can determine weaknesses in the power grid with minimal user inputs. Further, it can be used throughout the design flow to perform block-level power and signal EM analysis. Totem can also natively support digital place & route design components in mixed-signal designs and can combine several block-level views for full-chip analysis.

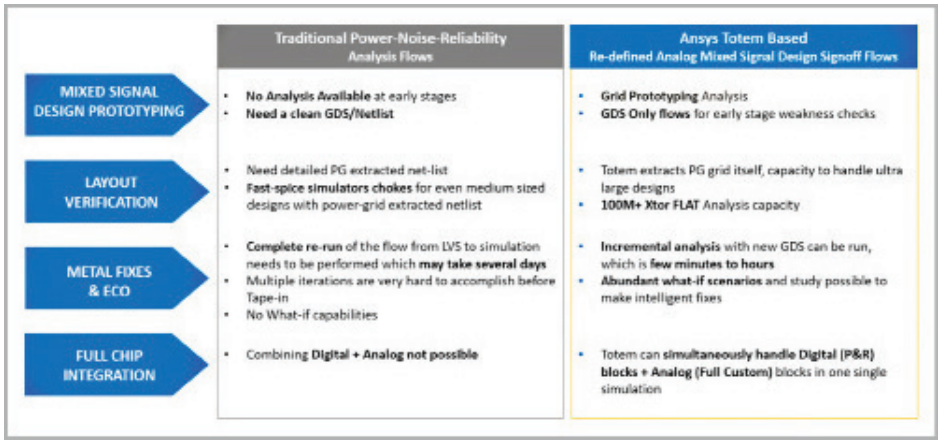

Figure 3: Redefining Analog Mixed Signal Design Signoff Flow with Totem

Advanced Analysis

Totem enables other advanced analyses like ESD integrity check, multiphysics workflows for PMIC including drain-source on-resistance (RDSON), and sensitivity analysis, guard ring weakness check, substrate noise injection analysis, transient power FET Analysis, and chip-package-system electrothermal analysis with Synopsys RedHawk-SC Electrothermal™ engine.

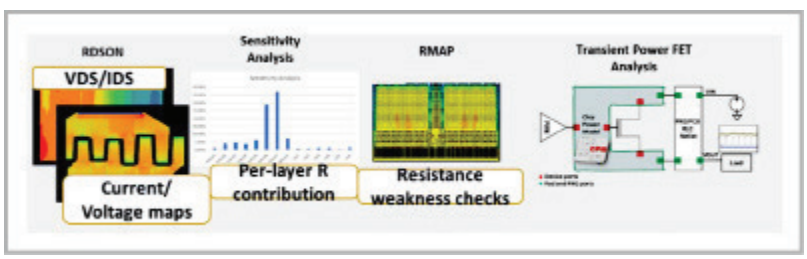

Figure 4: PMIC Analysis Using Totem Platform

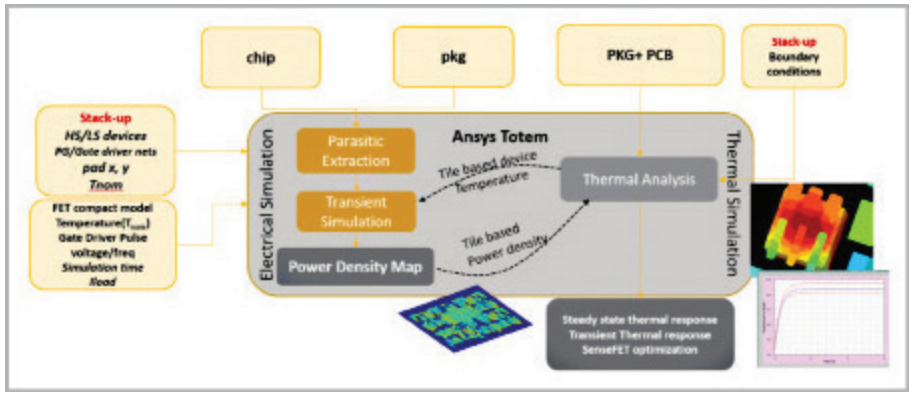

Figure 5: Totem PMIC Electrothermal Co-simulation

Synopsys Totem-SC

Synopsys Totem-SC™ is the next-generation analog mixed signal power noise signoff platform that builds on the Synopsys SeaScape™ platform to address the growing challenge of power integrity analysis facing today's extremely large memory and analog mixed-signal designs. SeaScape, the world's first custom designed big data architecture for electronic system design and simulation, provides per-core scalability, flexible design data access, instantaneous design bring-up, MapReduce-enabled analytics and many other revolutionary capabilities. Totem-SC delivers up to 10x faster performance on large designs for dynamic voltage drop signoff of next generation designs like complementary metal oxide semiconductor (CMOS) image sensors, dynamic random-access memories (DRAM), flash memories, field programmable gate arrays (FPGAs), and high-speed transceivers. Totem, the industry's leading solution for analog mixed signal power noise and reliability signoff is offered on the SeaScape platform as Totem-SC thus giving you the best of both worlds — the signoff confidence Totem provides and the elastic scalability and big data analytics of SeaScape.

Elastic Compute Scalability

Totem-SC shares core engines with the next-generation SoC power noise sign off platform, Synopsys RedHawk-SC. With unparalleled scalability across thousands of cores using big data techniques, Totem-SC can perform power and reliability signoff for analog and mixed signal design with extremely fast turnaround time on commodity hardware. Totem-SC runs the larger designs, using low memory cores, even if they reside on different machines. Totem-SC starts working as soon as a single core is available. It proportionately speeds up as more cores become available and has the resiliency to recover should any core or machine become unresponsive. Because Totem-SC can utilize unused cores, it increases utilization rates of compute farms, thereby decreasing overall hardware costs. Unlike other tools, it does not require dedicated hardware, even for the largest designs.

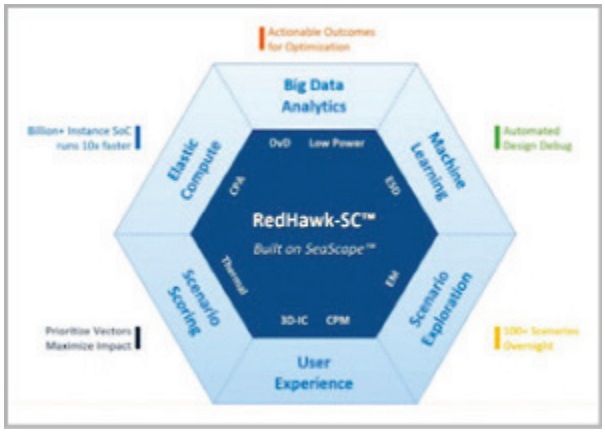

Figure 6: RedHawk-SC Platform

Big Data Analytics

Big data analytics enable rapid data mining and analytics to drive actionable outcomes and optimization. Using custom data analytics, you can identify and prioritize only those design fixes that are key to product success. Custom analytics powered by MapReduce enable you to query the largest designs in minutes.

Spice Accuracy

Totem-SC leverages the foundry-certified RedHawk-SC engine and accurately meshes wide metal shape and long via structures that enable correlation of dynamic voltage drop with Spice and Totem.

Unparalleled Capacity

Totem-SC can handle ultra-large, full GDS custom design with significant runtime acceleration of GDS and waveform processing by utilizing its highly distributed and scalable architecture. A fast and customizable user interface in Totem-SC has a persistent database with a thin client GUI and is able to perform advanced analytics and data-mining with powerful Python UI while providing the same look and feel of Totem.

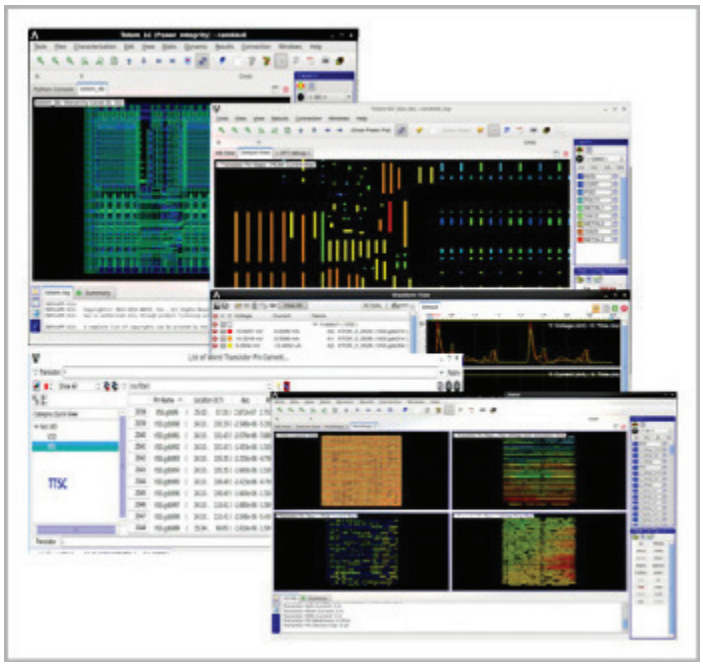

Figure 7: Totem-SC Fast and Debug Friendly GUI

Advanced Analysis

Totem-SC can perform 2.5D and 3D-IC power noise analysis. It also includes several new early analysis flows such as Build Quality Metric (BQM), Region Current Analysis (RCA), and Fast Reff for static voltage drop, giving users high confidence in signoff.

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