TestMAX SMS

Complete Memory Test, Repair and Diagnostics Solution

A comprehensive, integrated test, repair and diagnosis solution for embedded memories

Overview

TestMAX SMS is a comprehensive, integrated test, repair and diagnostics solution that supports repairable or nonrepairable embedded memories across foundry, process node and memory IP vendors. Its highly automated design implementation and diagnostic flow enables system-on-chip (SoC) designers to achieve quick design closure and significantly improve time-to-market and time-to-yield in volume production.

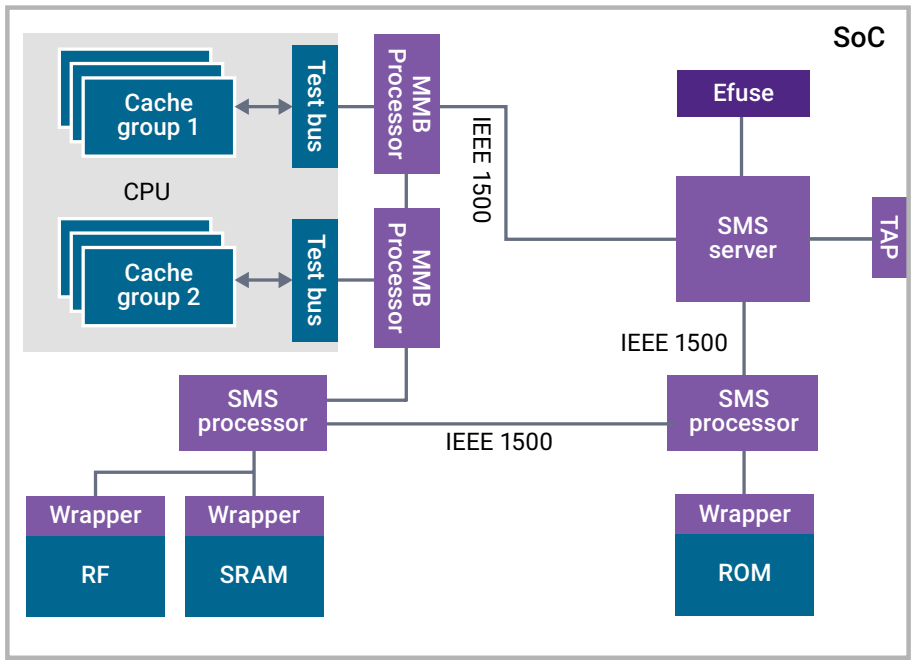

Figure 1: TestMAX SMS solution

Key Benefits

- Full RTL integration flow with TestMAX Manager
- Hierarchical architecture and automated SoC integration and verification
- High-quality test to provide full memory defect coverage with minimum test time
- High yield with efficient on-chip repair across multiple operating corners
- Superior diagnostics with physical failed bitmaps and XY coordinate identification to quickly determine root cause of failures

Key Features

- TestMAX SMS provides all the key elements for embedded memory test and repair utilizing the DesignWare® Self-Test and Repair (STAR) Memory System components:
  - STAR Memory System wrapper
  - STAR Memory System processor
  - STAR Memory System server and sub-server
  - MMB Processor for high performance cores
- Test algorithm programmability
- Tester patterns and diagnostics
- Silicon bring-up and characterization

High-Performance Core Support

TestMAX SMS allows at-speed test and repair of high-performance processor cores by using a preconfigured test bus, which provides access to the memories inside the core in test mode. TestMAX SMS uses this shared multi-memory bus (MMB) to test memories and add memory test and repair logic outside the IP core to avoid any impact on processor core performance.

Test Algorithm Programmability

TestMAX SMS provides full test algorithm programmability. The STAR Memory System processor includes a BIST module to execute test algorithms. The default test algorithms in the BIST module can be replaced with new algorithms in the RTL or in silicon, and the user can program either their own custom algorithms or select from the comprehensive library of algorithms provided with TestMAX SMS.

Tester Patterns and Diagnostics

The STAR Memory System Yield Accelerator addresses the need to rapidly, cost-effectively and accurately identify, analyze, isolate and classify memory faults as designs are readied for transition from first silicon to volume manufacturing. Leveraging the infrastructure of the STAR Memory System, the Yield Accelerator automatically generates vectors for test equipment and provides fault analysis and root-cause failure guidance based on silicon test results. Using this feature, test and product engineers can rapidly analyze failures manifested in embedded memories and inspect the physical location and class of each fault to determine the root cause without involving the IP vendor or SoC designer.

On-Chip Self-Repair

Unlike complex external repair flows, TestMAX SMS's on-chip repair is fully automated. A built-in self-diagnosis module determines the location of any memory defect and provides error logging by scanning out failure data for silicon debug. When testing memories with redundancies that have failures, a built-in repair and redundancy allocation module identifies available redundant elements and determines the best possible redundancy configuration.

Silicon Bring-up and Characterization

The STAR Memory System Silicon Browser has advanced automation capabilities to interactively communicate through a JTAG port with the STAR Memory System's infrastructure in a chip for post-silicon bring-up, system debug, diagnosis and characterization of embedded memories. The unique features of the Silicon Browser allow extraction of memory contents, multi-corner and multi-voltage characterization, precise physical failure localization, defect classification and redundancy utilization analysis, all from an engineer's desktop and without the need for expensive automatic test equipment.

Design Formats

TestMAX SMS supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Assertion: OVL, SV
- Verification: SAIF, VCD, FSDB