Overview

Synopsys TestMAX Manager extends DFT automation to the RTL implementation phase to provide a comprehensive RTL integration flow while extending into the system and field-testing domain.

TestMAX Manager provides a Tcl based framework for the interoperability of the Synopsys TestMAX family of products, enabling flow automation and customization along with design introspection and editing capability. Figure 1 provides a graphical overview of the Synopsys TestMAX product family.

Key Benefits

- Common interface for all DFT tools
- Full RTL flow integration support

Key Features

- Full RTL flow integration support
  - Test planning at RTL
  - RTL generation for memory test, XLBIST, codec, and OCC IP
  - Instantiates and connects DFT IP into the design RTL
  - RTL validation of connectivity and rule checks

Figure 1: Synopsys TestMAX product family overview
- Comprehensive RTL editing
- Hierarchical pattern porting
- Supports all compression technologies: DFTMAX, DFTMAX Ultra, DFTMAX SEQ, TestMAX XLBIST
- Merges multiple core patterns with full hierarchical support
- Generates verification testbenches at all hierarchical levels

**Full RTL flow integration support**

TestMAX Manager provides a complete, integrated RTL-to-ATE implementation and verification flow. Figure 2 shows an overview of the primary flow steps and processes.

![Flow Diagram](image)

**Design Formats**

TestMAX Manager supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Assertion: OVL, SV
- Verification: SAIF, VCD, FSDB

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