SYNOPSYS®

DATASHEET

TestMAX DFT

Design-for-Test Implementation

Comprehensive, advanced design-for-test (DFT)

Overview

Synopsys TestMAX DFT is a comprehensive, advanced design-for-test (DFT) tool that addresses the cost challenges of testing designs across a range of complexities. TestMAX DFT supports all essential DFT, including boundary scan, scan chains, core wrapping, test points, and compression. These DFT structures are implemented through TestMAX Manager for early validation of the corresponding register transfer level (RTL), or with Synopsys synthesis tools to generate netlists.

Multiple codecs and architectures are supported that address the need for ever-higher levels of test data volume, test time reduction, and fewer test pins.

TestMAX DFT leverages Synopsys Fusion Technology to optimize power, performance and area for the design, minimizing the impact from DFT.

Key Benefits

- Lowers test costs
- Enables high defect coverage
- Accelerates DFT validation using RTL
- Minimizes impact on design power, performance, and area
- Preserves low-power design intent
- Minimizes power consumption during test
- Integration and verification of IEEE1687 network and compliant IP
- Integration and verification of IEEE 1500 access network

Key Features

- High test time and test data reduction
- Patented, powerful compression technologies
- RTL generation with TestMAX Manager
- Fused into Design Compiler® and Fusion Compiler™ for concurrent optimization of area, power, timing, physical and test constraints

- Hierarchical scan synthesis flow support
- Pin-limited test optimizations
- Unknown logic value (X) handling
- Location-aware scan chain reordering during incremental compile
- Core wrapping with shared use of existing core registers near core I/Os
- Analysis-driven test point insertion using TestMAX Advisor
- Flexible scan channel configurations to support multi-site testing and wafer-level burn-in
- Multiple compression configurations to support different testers and packages with different I/O
- Boundary scan synthesis, 1149.1/6 compliance checking and BSDL generation
- Consistent, comprehensive DRC shared with ATPG
- Enables TestMAX ATPG for compressed pattern generation
- IEEE 1687 ICL creation and verification
- Hierarchical IEEE 1687 PDL pattern porting
- Automated pattern porting and generation of tester-ready patterns in WGL/STIL/SVF and post-silicon failure diagnostics

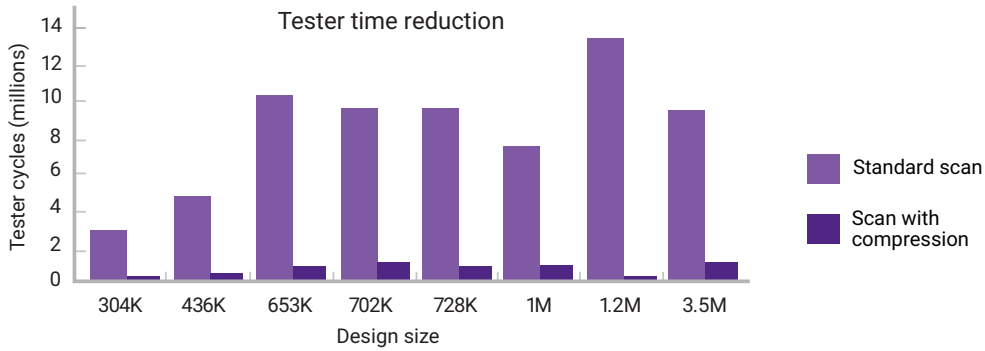

Figure 1: TestMAX DFT delivers high test time and test volume reduction

High Test Time and Test Data Reduction

TestMAX DFT reduces test costs by providing high test data volume compression (Figure1). Using Synopsys' patented TestMAX DFT compression architectures, TestMAX DFT saves test time and makes it possible to include high defect-coverage test patterns in tester configurations where memory is limited. With the industry's most area-efficient solution, TestMAX DFT has virtually no impact on design timing and results in the same high test coverage as provided by standard scan (Figure 2a). For additional test time and data reduction, TestMAX DFT implements test points within synthesis, via its transparent links to TestMAX Advisor for powerful test point analysis and selection.

Pin-Limited Test

To accommodate designs that require a limited number of test data pins either at the top-level or per core, TestMAX DFT generates an optimized architecture that ensures high quality without incurring extra test data. Several factors limit the number of available test pins, including tighter form factors, multi-site testing to target multiple die simultaneously, and core-based methodologies with multiple embedded compressor-decompressors (codecs). These types of techniques minimize the number of chip-level test pins available to each codec. To provide high test data volume and test application time reduction for these pin-limited test applications, TestMAX DFT generates a low-pin tester interface. Use TestMAX DFT to minimize the required number of scan I/O for pin-limited testing (Figure 2b).

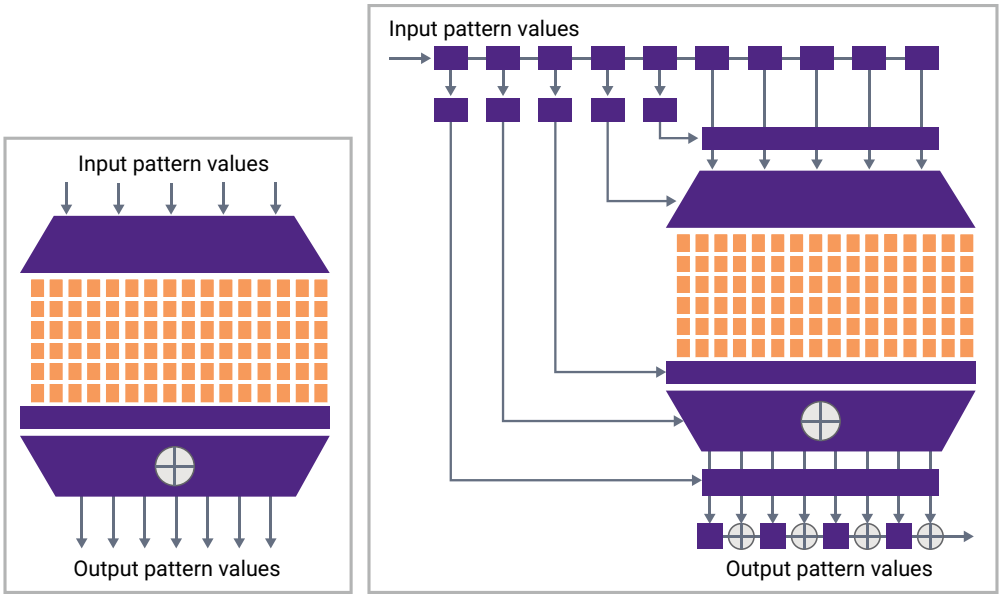

Figure 2a: (left) Codec optimized for high pin count; Figure 2b. (right) Codec optimized for pin-limited testing

DFT Implementation into RTL

In conjunction with TestMAX Manager, TestMAX DFT offers early validation of complex DFT logic and architecture by producing RTL. For easy adoption, commands are similar to Synopsys' widely deployed standard scan synthesis flow. TestMAX DFT generates compression logic directly into RTL, which can be verified with the VCS® simulator or other Verilog simulation tools. In addition, all test and design constraints are automatically generated for synthesis tools. Validation of RTL DFT ensures key compression logic and connections with other DFT logic such as logic BIST and memory BIST operate as specified, prior to synthesis, leading to very high and predictable test coverage and test compression results.

DFT Synthesis

The TestMAX DFT synthesis flow is based on the industry's most widely deployed standard test synthesis flow and incorporates Test Fusion technology. TestMAX DFT synthesizes DFT logic directly from RTL or gates into testable gates with full optimization of synthesis design rules and constraints. All test and compression requirements specified prior to the synthesis process are met concurrently with area, timing and power optimization. TestMAX DFT also enables TestMAX ATPG to seamlessly generate compressed test patterns while achieving high test quality.

Complete DFT Rules Checking

For maximum productivity, and prior to executing TestMAX DFT, TestMAX Advisor enables designers to create "test-friendly" RTL. TestMAX Advisor identifies DFT rules violations early in the design cycle during the pre-synthesis stage to avoid design iterations. Specifically, TestMAX Advisor validates that the design is compliant with scan rules to ensure operational scan chains and the highest test coverage. The violations can be diagnosed using its powerful integrated debugging environment that enables cross-probing among violations, RTL and schematic views. For flows within Design Compiler and Fusion Compiler products, TestMAX DFT provides comprehensive design rule checking for scan and compression logic operation.

Fusion Design Platform For Concurrent Optimization Of Area, Power, Timing, Physical And Test Constraints

With Synopsys' synthesis flow (Figure 3), scan compression logic is synthesized simultaneously with scan chains within the Fusion Design Platform. Location-based scan chain ordering and partitioning provides tight timing and area correlation with physical results using Fusion Compiler or IC Compiler. This enables designers to achieve area, power, timing and DFT closure simultaneously. TestMAX DFT writes detailed scan chain information which Synopsys' physical design tools read, which then perform further optimizations to reduce area impact and decrease overall routing congestion (Figure 4).

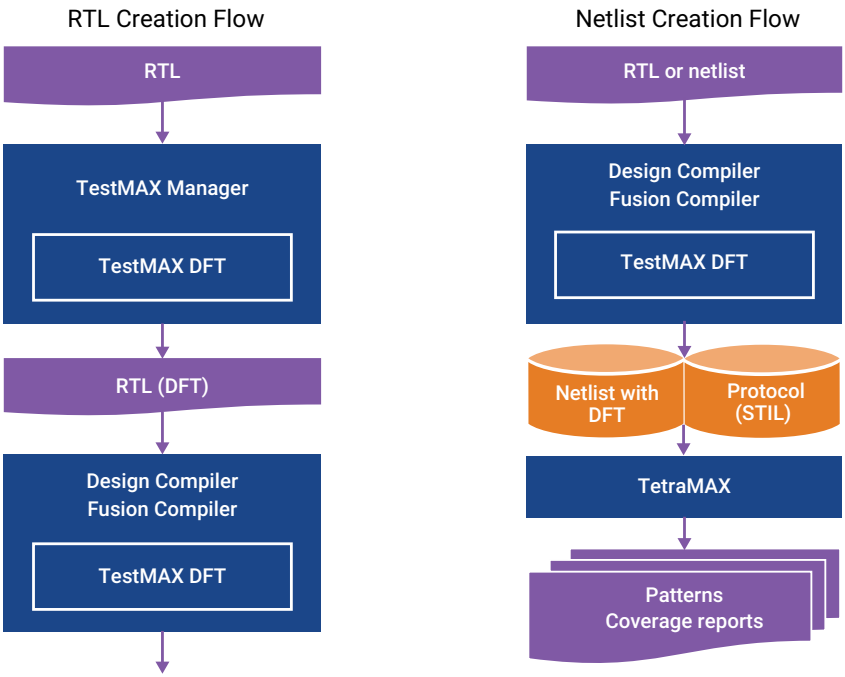

Figure 3: Test compression flow

Integrating DFT resources into a complex multi-voltage design can be a time-consuming and error-prone process without automation tailored for low-power flows. Once voltage domain characteristics of the design with IEEE 1801 (unified power format or UPF) are specified, TestMAX DFT automatically inserts level shifters and isolation cells during scan chain implementation. To reduce routing congestion and area impact of the DFT logic, TestMAX DFT minimizes both scan chain crossings between power/voltage domains and the number of level shifters inserted.

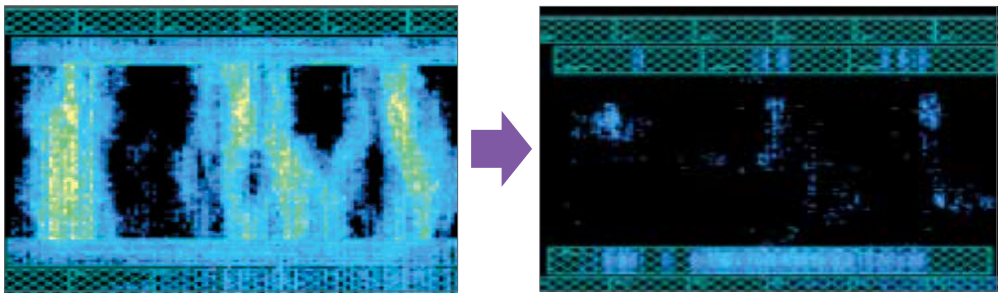

Figure 4: These screen captures show TestMAX DFT results without the routing congestion associated with standard scan

Hierarchical Scan Synthesis

To handle test synthesis of very large designs, some level of abstraction is required so that the system/chip integrator can reduce design time. By abstracting the DFT information in a test model, along with timing and placement information, TestMAX DFT enables quick hierarchical test implementation of multi-million gate designs.

Boundary Scan Synthesis and Compliance Checking to the 1149.1/6 Standard

TestMAX DFT delivers a complete set of boundary scan capabilities including:

- TAP and BSR synthesis
- Compliance checking to the IEEE 1149.1/6 standard
- Boundary Scan Description Language (BSDL) file generation
- Functional and DC parametric pattern generation for manufacturing test

Integrated Setup of TetraMAX ATPG for Pattern Generation

TestMAX DFT transfers all information about the scan compression architecture and test operation to TestMAX ATPG. Working together, TestMAX ATPG and TestMAX DFT automatically generate compressed, power-aware test patterns with highest test coverage.