SYNOPSYS®

DATASHEET

TestMAX Advisor

RTL Testability Analysis and Optimization

Design-for-test rule checking and RTL fault coverage estimation capabilities that help designers pinpoint testability issues early in the flow

Overview

Synopsys TestMAX Advisor, built on SpyGlass® technology, performs RTL testability analysis and optimization, enabling designers to fine-tune RTL early in the design cycle to predictably meet manufacturing and in-system test coverage goals. The tool's extensive design-for-test (DFT) rule checking and RTL fault coverage estimation capabilities pinpoint testability issues early in the flow (Figure 1) thereby enabling designers to avoid test bottlenecks downstream that can lead to time-consuming design iterations. TestMAX Advisor identifies areas in the design with hard-to-test ATPG faults and provides a report of test points to improve test coverage and reduce patterns and test costs.

TestMAX Advisor can also be used with TestMAX Manager in the RTL creation flow (Figure 2), where all of the TestMAX DFT can be inserted and verified at the RTL design stage by TestMAX Manager and all resulting new connectivity can be verified by TestMAX Advisor.

Key Benefits

- Shortens test implementation time and cost by ensuring RTL or netlist is scan-compliant
- Improves test quality by diagnosing DFT issues early at RTL or netlist

Key Features

- Lint checking and analysis for DFT
- Connectivity and IP rule checks
- Test Point selection for hard-to-test faults
- RTL stuck-at and transition fault coverage estimation
- Intuitive, integrated debug environment with cross-probing among views

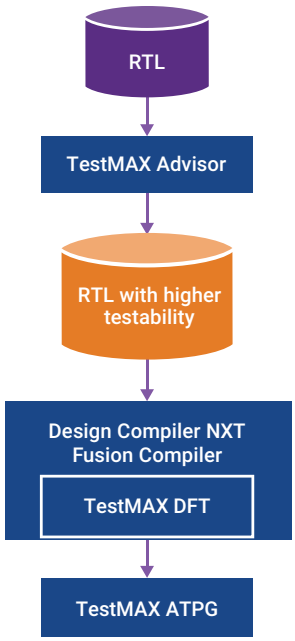

Figure 1: TestMAX Advisor addresses testability issues early in the design flow

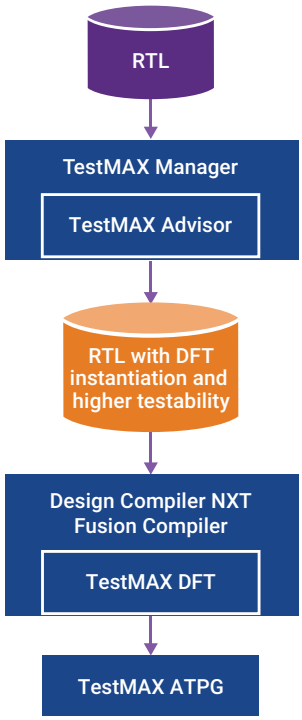

Figure 2: TestMAX Advisor in RTL creation flow

Lint Checking and Analysis for DFT

TestMAX Advisor performs lint checking to ensure the RTL or netlist can achieve maximum ATPG coverage. The tool verifies that the design meets scan DRC requirements, providing detailed audit reports that help designers identify missing test constraints and make appropriate modifications to the design to address scan issues. It also verifies that a multi-voltage design complies with low-power DFT rules. For example, one type of check ensures that low-power constraints are compatible with scan test requirements; another type, applicable to netlists, verifies that scan chains do not cross voltage domains without level shifters.

Checking for Test Robustness

Testability profiling assesses test robustness—the susceptibility of test patterns to electrical glitches—and identifies RTL constructs that limit maximum stuck-at and transition fault coverage. Rule violations always reference the RTL so that designers know exactly where to make changes. To easily diagnose testability issues in the RTL, TestMAX Advisor provides an intuitive, integrated debug environment that enables cross-probing among views (Figure 3).

Random Pattern Analysis

A fault is deemed hard-to-detect if it has a very low probability of detection in a test composed entirely of randomly generated patterns. TestMAX Advisor analyzes random pattern coverage to identify hard-to-detect faults and suggests changes to meet testability goals. The random pattern coverage estimation is displayed in a hierarchical fault browser.

Designers can quickly zoom into the blocks that have significant low coverage and further analyze which portion of the design leads to poor coverage.

Uncovering at-Speed Test Issues

Resolving at-speed test issues at the RTL can save weeks of effort. TestMAX Advisor identifies timing closure issues caused by at-speed tests, which often achieve lower fault coverage than required even when full-scan is utilized, and the stuck-at coverage is high. The following are examples of at-speed rules in TestMAX Advisor that identify issues related to both timing closure and low coverage:

- PLL reference clock controllable from root level ports
- PLL control inputs controllable from root level ports
- All flip-flops controllable by PLL in at-speed test mode
- Asynchronous logic in the functional mode should not interact synchronously in test mode
- Synchronous logic in the functional mode should not interact asynchronously in test mode
- Required frequencies must be achievable

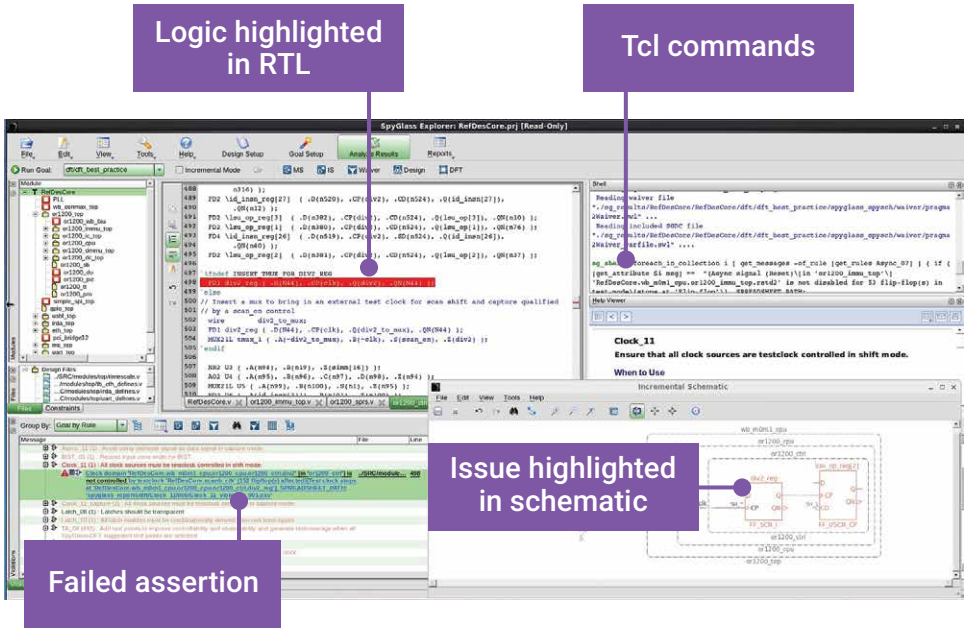

Figure 3: Integrated debug environment enables cross-probing among views to easily diagnose testability issues

RTL Fault Coverage Estimation

TestMAX Advisor provides estimates of stuck-at and transition delay fault coverage based on controllability and observability analysis. Coverage estimates are quick and pattern-less, thereby avoiding testbenches or long runtimes. Audit reports provide step-by-step guidance that allows designers to quickly and incrementally isolate the source of coverage loss.

Connectivity Validation

TestMAX Advisor validates connectivity across hierarchies checking both paths and values. This validation not only applies for test logic added at SoC integration level but also for any logic not related to test. TestMAX Advisor addresses connectivity challenges such as back-to-back on-chip controllers (OCCs) that find no clock control connection. Examples of value checks include PLL resets or clock gating enable pins. Conditional checks are also supported, for example memory sleep controlled by pin at IP level. Connectivity validation can be performed either at RTL or gate-level netlists.

Test Points Selection

Some of the faults in the design are ATPG testable but difficult to test. TestMAX Advisor identifies hard-to-test areas in the design and reports an ordered list of test points that can be inserted at hard to control and observe points to improve test coverage and reduce pattern count. The test points identified by TestMAX Advisor can then be inserted by TestMAX DFT. To reduce area congestion, physically-aware test points are supported where physical information about the test points selected by TestMAX Advisor can be used by Design Compiler® NXT and Fusion Compiler™ (as shown in the Synopsys design flow in Figure 1 and Figure 2). Test points are grouped based on physical data, allowing one flop to be shared across multiple test points, resulting in significant area overhead reduction.

Reference Methodology

The TestMAX Advisor reference methodology provides a structured, easy-to-use, and comprehensive process for resolving RTL design issues, thereby ensuring high quality RTL with fewer design bugs. The methodology leads to fewer but more meaningful violations, thus saving time for the designer. The methodology documentation and rule sets are provided with TestMAX Advisor.

Design Formats

TestMAX Advisor supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Verification: VCD, FSDB

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