SYNOPSYS®

DATASHEET

TestMAX ATPG

Advanced Pattern Generation

State-of-the-art pattern generation for unparalleled runtime

Overview

Synopsys TestMAX™ ATPG is Synopsys' state-of-the-art pattern generation solution that enables design teams to meet their test quality and cost goals with unprecedented speed. It delivers unparalleled runtime, ensuring patterns are ready when early silicon samples are available for testing. In addition, it generates significantly fewer patterns than existing solutions, allowing designers to reduce the time and cost of testing silicon parts, or increase test quality without impacting test cost. TestMAX ATPG is integrated with Synopsys' patented TestMAX DFT.

Key Benefits

- Generates high-coverage test patterns in hours instead of days
- Lowers test time and cost with fewer patterns than existing solutions
- Enables highly efficient utilization of hardware resources for ATPG
- Ensures easy, risk-free deployment into design and test flows

Key Features

- Highly optimized, memory-efficient test generation, and fault simulation engines for order-of-magnitude faster ATPG runtime compared to previous technologies
- Fine-grained multithreading across multiple cores overcomes memory bottlenecks
- Identical test coverage and pattern reduction across different server configurations and machines for consistent analysis
- Production-proven rule checking, design modeling, and fault modeling for easy, risk-free deployment
- Integration with TestMAX Diagnosis for consistency with defective silicon diagnostic results
- Advanced fault models for achieving extremely high test quality, standard and slack-based transition, cell-aware, static/dynamic bridging, path delay, and hold-time
- Interfaces with PrimeTime®, StarRC™, and HSPICE® for easy access to physical and timing data used by the models
- IDDQ pattern generation and validation using VCS® for quiescent state testing
- Power-aware pattern generation for limiting power consumption during shift and capture

Unparalleled ATPG Runtime

Increasingly complex SoC designs and shrinking schedules require fast ATPG turnaround time. Even though compute servers have multiple cores available for pattern generation, the cores are often under-utilized because existing ATPG technologies require a large amount of memory per core, effectively limiting the number of cores that can actually be used.

TestMAX ATPG overcomes this memory bottleneck using state-of-the-art test generation engines (Figure 1) that are extremely fast, exceedingly memory-efficient, and highly optimized for fine-grained multithreading of ATPG processes across multiple cores. The core engines have been designed to surpass previous technologies that are limited by high memory usage, enabling TestMAX ATPG to achieve higher core utilization (Figure 2) and 10X faster runtime (Figure 3).

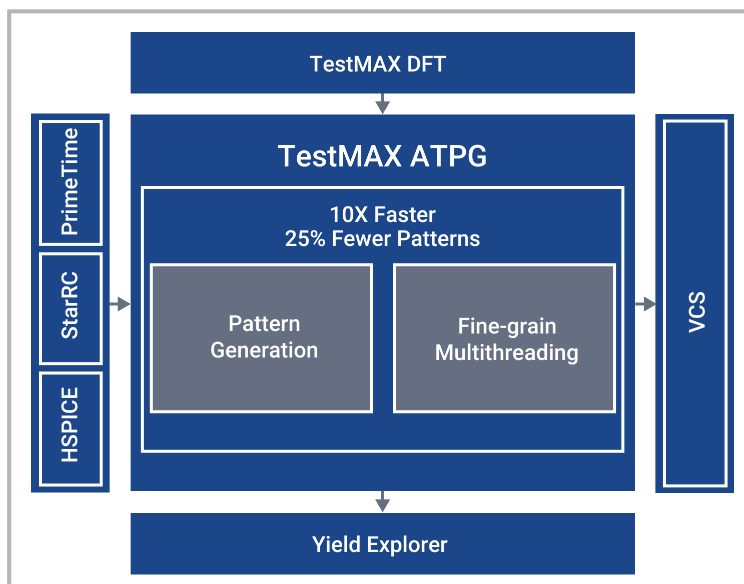

Figure 1: TestMAX ATPG is built on state-of-the-art engines to dramatically improve runtime and pattern count, while the rule checking, design and fault modeling infrastructure, and tool interfaces are unchanged

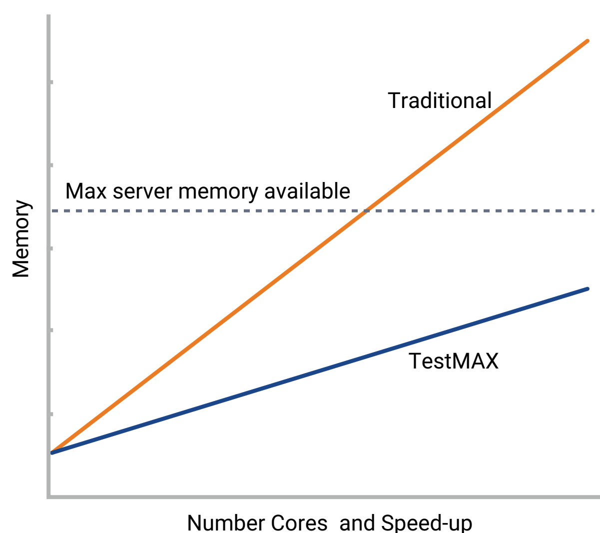

Figure 2: TestMAX ATPG eliminates memory bottlenecks and speeds-up ATPG as cores are added

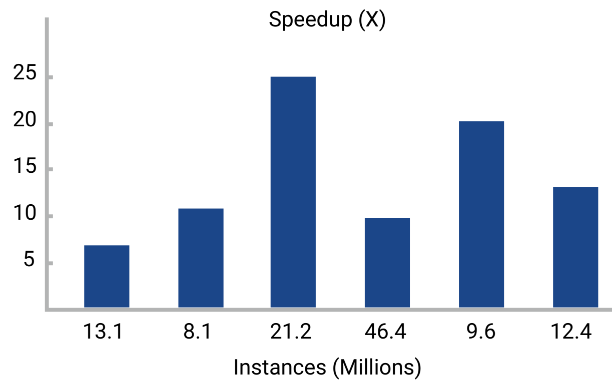

Figure 3: TestMAX ATPG runtime speedup compared to TetraMAX ATPG for different designs

25% Fewer Test Patterns

Decreasing pattern count reduces test time and cost or, depending on design requirements, facilitates an increase in test quality for the same cost. Algorithmic advances in TestMAX ATPG enable detection of more faults per pattern than existing methods, resulting in 25% fewer patterns on average (Figure 4). Multi-fault pattern optimizations also ensure that the default ATPG settings produce virtually the smallest pattern set. Moreover, TestMAX ATPG generates the identical compact pattern set bit-for-bit regardless of the number of cores used, facilitating easy QoR analysis and pattern debug across different server configurations and machines.

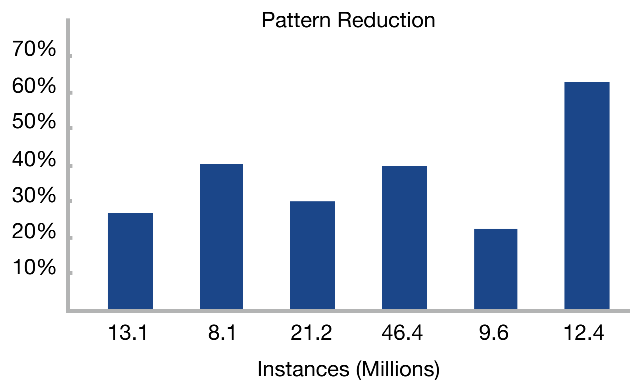

Figure 4: TestMAX ATPG pattern reduction compared to TetraMAX ATPG for different designs

Easy, Risk-Free Deployment

TestMAX ATPG is fully compatible with the legacy TetraMAX ATPG products and supports the same production-proven capabilities, allowing designers to quickly deploy it risk-free on their most challenging designs. Although it is built on engines that dramatically improve runtime and pattern count, the rule checking, design and fault modeling infrastructure, and tool interfaces are unchanged.

TestMAX ATPG's powerful design rule checker (DRC) supports full scan and partial scan test methodologies using mux-scan, clocked-scan, level sensitive scan design (LSSD), and proprietary schemes. For maximum flexibility, TestMAX ATPG accepts user-defined constraints and initialization patterns required for proper scan chain shifting. Complete support is provided for designs with IEEE 1149.1/6 internal scan shifting protocols and related techniques that minimize the number of external I/O pins required for ATPG.

Advanced Fault Modeling

TestMAX ATPG offers additional functionality that includes advanced fault modeling, IDDQ testing, and power-aware pattern generation. Many manufacturing defects will not be caught without additional high defect-coverage tests that specifically target subtle nanometer defects to further reduce defective parts per million (DPPM). TestMAX ATPG utilizes advanced fault models such as standard and slack-based transition, cell-aware, static bridging, dynamic bridging, path delay, and hold-time to generate high defect-coverage test patterns. Some of these models use data generated by other Design Fusion tools (Table I). For example, cell-aware models leverage physical data from StarRC extraction and detailed timing information from HSPICE simulations for TestMAX ATPG to target timing-critical defects inside cells.

Fault Model	Fusion Design Platform Tool
Bridging	StarRC
Path delay	PrimeTime
Hold-time	PrimeTime
Slack-based	PrimeTime
Cell-aware	StarRC, HSPICE

Table 1: ATPG fault models and the tools that create physical or timing data for the models

IDDQ Testing

TestMAX ATPG generates a minimal set of high fault coverage patterns for IDDQ testing purposes and constrains the test patterns to avoid excessive current during the quiescent state. It then accurately validates these patterns for low quiescence using Synopsys VCS or other Verilog simulator, thereby ensuring the IDDQ patterns will function on the ATE.

Power-Aware ATPG

Scan testing typically increases transistor switching activity by many times their peak functional-mode levels, leading to excessive power consumption. Too much power consumption during test can lead to the failure of good devices on the tester and unnecessary yield loss. TestMAX ATPG limits power consumption during scan and capture by automatically reducing switching activity to levels consistent with normal operation, based on designer-specified power budgets. Power reduction is achieved without compromising test coverage.

TestMAX ATPG also supports hardware-assisted shift power reduction, which decreases average shift power and pattern count compared to an ATPG-only approach through the use of independently controlled scan chain groups implemented with TestMAX DFT.

Tight Links with Synopsys Tools

TestMAX ATPG utilizes established interfaces with Synopsys Fusion tools and other Synopsys tools to deliver the highest quality test and the fastest, most productive flows:

- Integrated with TestMAX DFT, which is built into TestMAX Manager, Design Compiler® NXT and Fusion Compiler™ tools to provide early validation and optimize timing, power, area, and congestion for test as well as functional logic
- TestMAX XLBIST for self-test applications that require powerful and flexible X tolerance
- Integrated with TestMAX Diagnosis and Yield Explorer for seamless volume diagnostics and yield analysis to uncover design and process issues causing yield loss
- Guided by slack data from PrimeTime to accurately target timing-critical defects
- Leverages physical data from StarRC extraction and detailed timing information from HSPICE simulations for cell-aware ATPG that targets timing-critical defects inside cells

Netlist and Test Pattern Formats

TestMAX ATPG supports the same industry standards for data formats, simulation testbenches, and tester interfaces:

- Circuit netlist: Verilog, VHDL (1987 and 1993)
- Library: Verilog functional (Structural and UDPs)
- Timing exceptions: Synopsys Design Constraints (SDC)
- Simulation testbench: Verilog (serial and parallel)
- Test Patterns: STIL, WGL, Verilog

SYNOPSYS®
Silicon to Software™

©2019 Synopsys, Inc. All rights reserved. Synopsys is a trademark of Synopsys, Inc. in the United States and other countries. A list of Synopsys trademarks is available at synopsys.com/copyright.html. All other names mentioned herein are trademarks or registered trademarks of their respective owners.
03/08/19.CS321617153_TestMAX ATPG DS.