SYNOPSYS®
Accelerating Innovation

Synphony Model Compiler

Productivity for FPGA & ASIC Signal Processing

Faster and More Efficient Hardware Development for DSP Algorithms

Model-based design environments are popular for DSP algorithm design and exploration because they allow concise representation of behavior at very high levels of abstraction. These environments provide fast design capture and easy-to-use simulation and debugging tools. However, problems arise when the designer needs to translate the DSP design intent into hardware optimized for ASIC or FPGA implementation. Hand-coding RTL for DSP algorithms is very time consuming and can be error prone, resulting in tedious re-verification of the design in the RTL domain. Furthermore, hardware architecture exploration for area, delay, and power trade-offs is limited because of these difficulties. The Synphony Model Compiler solution addresses these problems by providing an easy and automated way to create ASIC and FPGA hardware from high-level models created in the Simulink and MATLAB® model-based environment.

High-Level Signal Processing IP Library

Synphony Model Compiler (SMC) provides a comprehensive, high-level model library for creating math, signal processing, and communications designs in the Simulink® environment. The library makes it very easy to capture fixed-point, multi-rate algorithms and optimize/debug their precision. The SMC library supports vector and matrix notation, which enables quick and concise capture of large multi-channel or highly parallel algorithms. The SMC library includes a powerful blockset designed for Giga Samples Per Second (GSPS) throughput designs, as well as a target-independent floating point blockset designed for efficient implementation on both FPGA as well as ASIC hardware.

SMC saves months in design and verification of signal processing hardware and systems with:

- A signal processing IP library
- Optimizations for QoR across multiple technologies, IP and system architectures
- High-performance verification for RTL and C-model system simulation

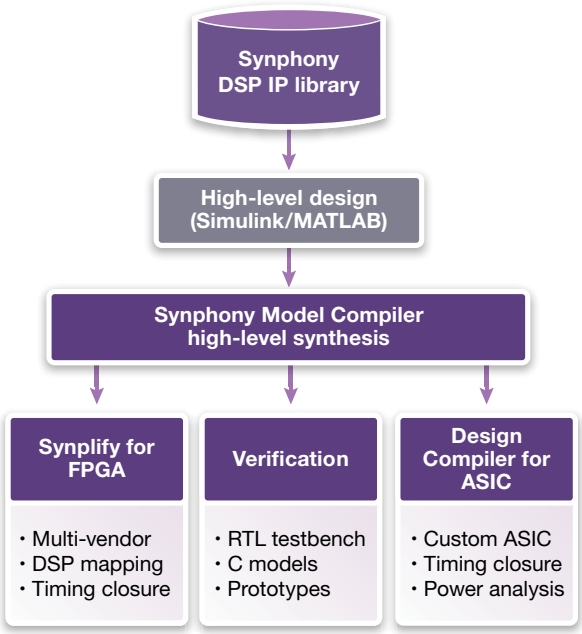

Figure 1: Synphony Model Compiler saves months in design and verification of signal processing hardware and systems

Blockset for GSPS Processing

Throughput in excess of achievable clock frequency is rapidly becoming a common design feature in various Military/ Aerospace and Instrumentation signal processing systems. Many SIGINT/ELINT/ COMINT systems require a blockset that can achieve GSPS throughput for common DSP algorithms such as FFT, FIR, CIC, NCO, and DDC. SMC includes a powerful set of parallel processing blocks that are designed to achieve GSPS throughput on both FPGA as well as ASIC hardware for common DSP algorithms.

Hardware Optimizations, Exploration, and Verification

Using a verified Synphony Model Compiler model, the RTL generation engine automatically creates RTL for hardware implementation and enables rapid exploration of architecture for area, power, performance, and throughput tradeoffs. This not only achieves higher design productivity but also reduces errors and risk by maintaining consistent verification across multiple architecture choices and target technologies. The SMC engine also includes advanced technology characterizations that utilize the Synopsys Synplify Premier® or Design Compiler® implementation products to make device-specific optimizations for the FPGA and ASIC targets, respectively.

C-Output for Faster System Simulation and Easier System Validation

Developing ASIC and FPGA hardware blocks often requires a significant system-level integration, simulation and validation effort. Model-based design environments are notoriously inefficient for running long simulations to validate functionality. Synphony Model Compiler significantly improves the productivity of system validation by automatically creating C-based models of the SMC RTL output. This eliminates the difficult and time-consuming effort of creating models by hand. SMC C-model generation is very flexible and creates high-performance, fixed-point ANSI-C models that can be used in a variety of system simulation environments including Simulink, SystemC, and RTL simulators such as Synopsys' VCS® and Mentor Graphics®' ModelSim®. The SMC C-models can be used in the model-based design environment to provide orders of magnitude simulation speedup and dramatically reduce the time required to validate the DSP algorithm.

For the first time, Synphony Model Compiler brings these capabilities together in a single environment that supports complete, integrated solutions with Synopsys' FPGA implementation, ASIC implementation, prototyping, and verification flows.

Improve Time-to-Market and Reliability

Synphony Model Compiler can shorten algorithm hardware design cycles by as much as 70% especially when optimized implementation and FPGA/ASIC technology portability are required. Design teams can validate algorithm concepts earlier in the design cycle, catch functional and system-level problems earlier, and explore design space tradeoffs more rapidly. With a rich library of powerful signal processing IP, automated hardware generation, and validation using higher levels of abstraction, system and algorithm designers can achieve higher productivity, reliability, and time-to- market in their ASIC and FPGA projects.

For more information about Synphony Model Compiler, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.

Features	Features
Synthesizable fixed-point, high-level IP model library	• Broad set of signal processing functions for wireless and communications applications • Multi-rate support • Vector and matrix support for fast creation of large multi-channel or parallel algorithms • Up to 128-bit precision (most blocks) • Fixed-point analysis and debugging support (min/max and overflow logging) • Synthesizable and optimizable using high-level synthesis implementation flow
Multi-rate algorithm design	• Broad high-level, multi-rate library support • High-level synthesis optimizations across multiple sample rates • Clock circuit generation and management of clocking strategies
GSPS processing	• Parallel input FFT, FIR, CIC, NCO blocks for Giga Samples Per Second (GSPS) processing • Optimized to provide throughput many times higher than the max clock frequency achievable in hardware
Floating point blockset	• Complete blockset for floating point arithmetic applications • Support for IEEE single precision, IEEE double precision, and custom precision
RTL encapsulation support	• Use RTL within your high-level SMC model • High-performance simulation with no external RTL simulators required • Easily add state machines, control logic, and cycle-accurate interfaces to your high-level SMC model • Easily use 3rd party IP in your high-level SMC model
Automatic RTL generation	• Target-aware optimizations for FPGAs and ASICs
HLS subsystems	• Partition designs into a hierarchy of HLS-optimizable subsystems • Verify top-level designs using high-level simulation and debugging • Independently apply and tune HLS optimizations for different subsystems • Scale the HLS flow for larger designs with higher quality of results
ASIC flow integration	• Automatic generation of RTL constraints and scripts for Design Complier • Advanced timing estimation using Design Compiler • Rapid architecture exploration of speed, area, and power tradeoffs
FPGA flow integration	• Automatic generation of RTL constraints and scripts for Synplify Pro®, Synplify Premier • Advanced timing estimation using Synplify Pro, Synplify Premier • Optimized resource mapping to advanced FPGA devices including hardware multipliers, MACS, adders, memories, and shift registers
RTL testbench generation	• Automatic generation of text vectors and scripts for RTL verification in VCS
C-model generation	• C-model creation for fast system-level validation and simulation • Cycle-accurate with the post-optimized RTL output • High-performance simulation: over 100X faster than RTL simulation • Automatic wrapper generation for various simulators including Simulink, VCS, ModelSim, and generic ANSI-C direct executable simulators

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