SYNOPSYS®
Predictable Success

StarRC Custom

Parasitic extraction for next-generation custom IC design

Overview

StarRC™ Custom is the advanced parasitic extraction solution architected for next-generation custom digital, analog/mixed-signal (AMS) and memory IC designs and IP characterization. A key component of the Synopsys Galaxy™ Implementation Platform, it is built on Synopsys' gold standard extraction engines including the brand new Rapid3D fast field solver technology. StarRC Custom expands Synopsys' custom design portfolio consisting of leading products such as Galaxy Custom Designer™ mixed-signal implementation solution, IC Validator physical verification solution, and CustomSim™ and HSPICE circuit simulation solutions.

StarRC Custom Solution

The convergence of computing, consumer, mobile and wireless multimedia applications necessitates integrating complex custom digital and analog functions in today's advanced system-on-chip (SoC) designs. However, the widespread use of custom IP is creating increased design and analysis bottlenecks for the design teams. Increasing transistor counts, process variation and the emergence of new parasitic effects at advanced technologies are exacerbating the accuracy and performance concerns associated with high-sensitivity custom designs. IC designers need a comprehensive parasitic extraction solution to address the exceptional challenges of critical custom circuits in their designs.

StarRC Custom addresses the needs of the next-generation custom IC designers by offering unified gold standard extraction engines, including the ScanBand™ pattern-matching technology and the new Rapid3D fast field solver technology, into a single solution. The combination of the two technologies enables StarRC Custom to deliver high performance with tuned accuracy to meet the stringent demands of the custom designs. In addition, StarRC Custom's comprehensive offering including the seamless integration with Galaxy Custom Designer and optimized links with CustomSim simulator, enable increased designer productivity in implementation and simulation analysis resulting in overall faster time-to-tapeout (see Figure 1).

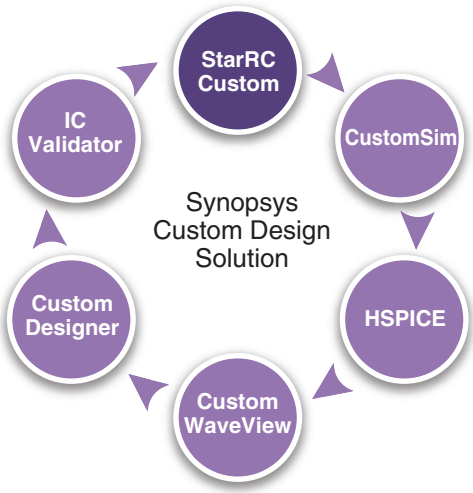


Figure 1: StarRC Custom is a key component of Galaxy Implementation Platform and Synopsys' custom design portfolio

Benefits

- Built on proven StarRC ScanBand™ extraction technology offering high performance, sub-femto Farad signoff accuracy and broadest qualification and usage in the industry
- Rapid3D fast field solver extraction delivering 20x speed improvement with atto Farad 3D extraction
- Advanced parasitic modeling, including silicon-accurate layout dependent (context-specific) device parasitic extraction for high-sensitivity custom circuits
- Highly optimized links with CustomSim circuit simulation delivering up to 10x simulation runtime acceleration
- Integration with Synopsys Galaxy Custom Designer and standard interface with third party custom design solutions for increased productivity

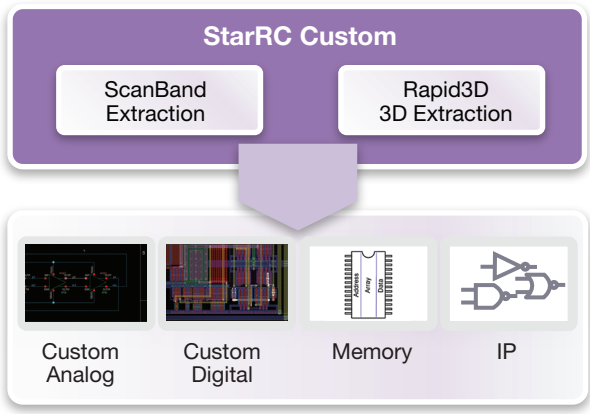


Figure 2: The unified gold standard extraction in StarRC Custom delivers high accuracy and performance for custom IC designs

Unified Gold Standard Extraction

For timing-sensitive circuits, such as critical nets, memory, AMS/RF, high-speed digital and other custom IP, accuracy is a non-negotiable design criterion. Designers generally require higher accuracy for such critical IP and circuits compared to the rest of the design but without severely impacting the overall turnaround time. In the StarRC Custom product, Synopsys' gold standard pattern-matching and 3D extraction technologies have been unified into a single solution (see Figure 2). The trusted sub-femto Farad accuracy of ScanBand technology is the foundation of the StarRC Custom solution providing the signoff accuracy and performance. The 3D field solver extraction technology brings more flexibility to the solution, especially for circuits where higher accuracy 3D self and coupling capacitance extraction is needed. The combination of the two technologies allows StarRC Custom to easily tune the extraction for targeted accuracy and productivity, as needed by the designers.

Rapid3D Extraction

Building on the Raphael NXT engine, the brand new Rapid3D technology incorporates the latest advancements in field solver algorithms to deliver 20x faster 3D extraction with 6x higher capacity while providing the same gold standard accuracy. It accounts for all 3D effects associated with the complex geometries of interconnect structures at sub-45-nm nodes for silicon accurate extraction that is tightly correlated with Synopsys' Raphael™, the reference field solver used by the major foundries.

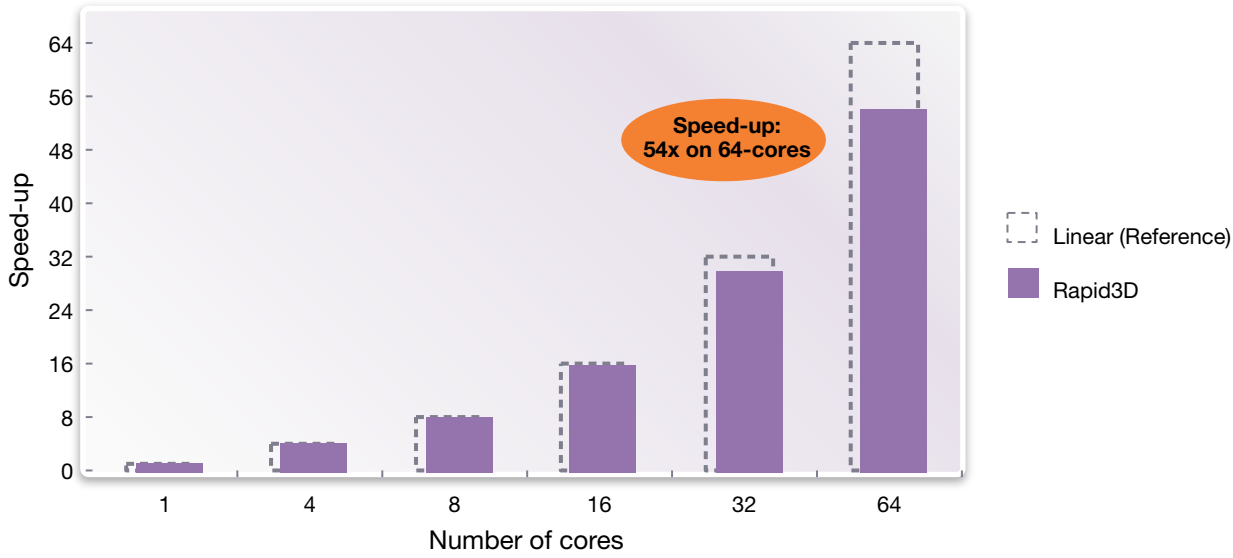
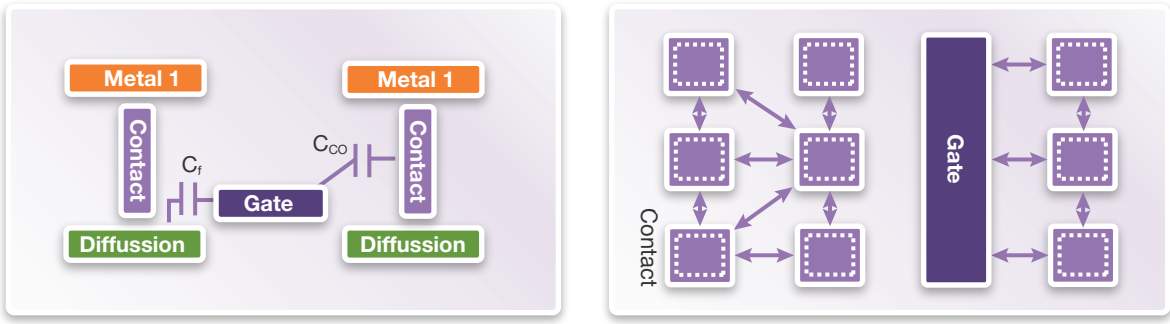


Figure 3: Rapid3D offers 20x faster 3D extraction on single core and additionally near linear multicore scalability delivering up to 54x speed-up on 64-cores



(a) Gate-to-contact, gate-to-diffusion capacitance

(b) Contact etch modeling

Figure 4: StarRC Custom's advanced parasitic modeling provides signoff accuracy

Rapid3D's modern architecture also includes multicore technology that demonstrates the performance scalability of up to an additional 54x speed-up on 64 processor cores. This allows designers to apply 3D extraction to a wide range of custom designs consisting of 10s to 100s of thousands of nets. In addition, the multicore technology supports efficient multi-threading that maximizes the throughput on memory-constrained compute resources.

The Rapid3D technology is embedded as a standard feature in StarRC Custom, providing users proven reliability, most advanced process modeling and standard interfaces to achieve the targeted silicon-accuracy and productivity. The seamless integration allows the Rapid3D technology to be used for high accuracy extraction to drive multiple custom implementation and analysis applications, such as standard cell characterization with Liberty NCX, custom layout with Galaxy Custom Designer, circuit simulation with CustomSim and HSPICE and signal integrity signoff with NanoTime.

Advanced Parasitic Modeling

Increasing process variation and new parasitic effects introduced at each new generation of process technology are significantly increasing design challenges, particularly for high-sensitivity custom designs. Advanced process technologies are elevating a variety of physical effects once

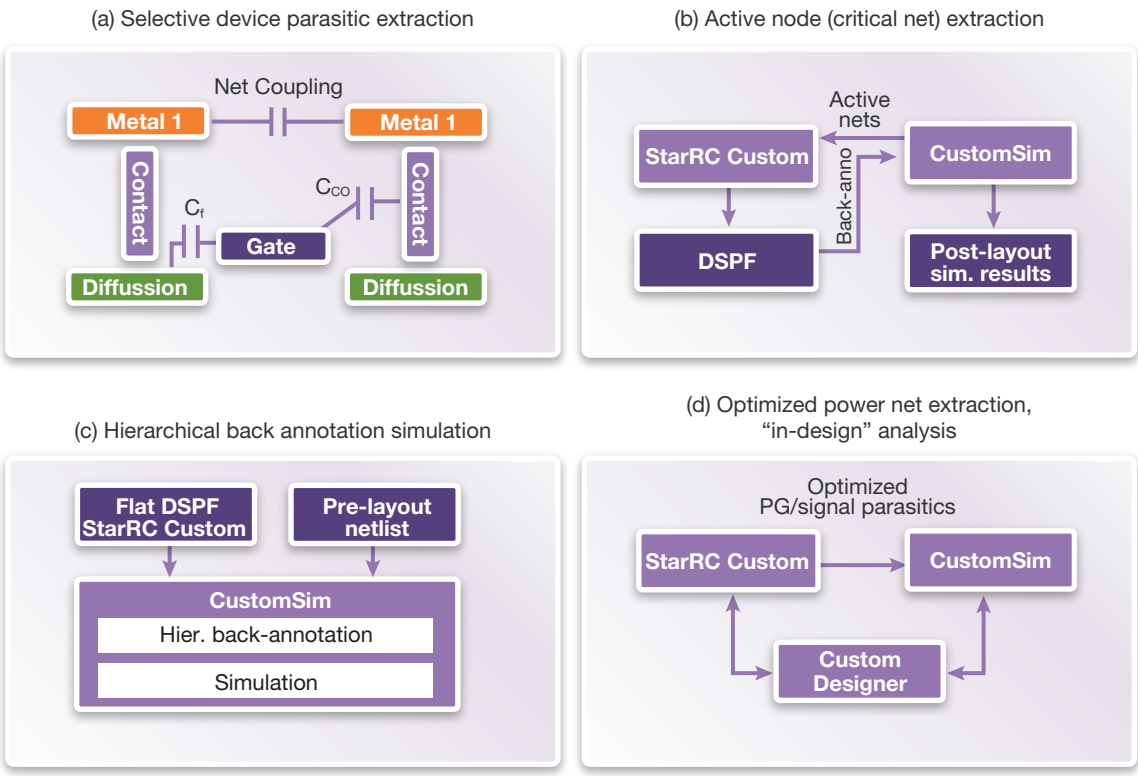


Figure 5: StarRC Custom's highly optimized links with CustomSim offer increased simulation performance

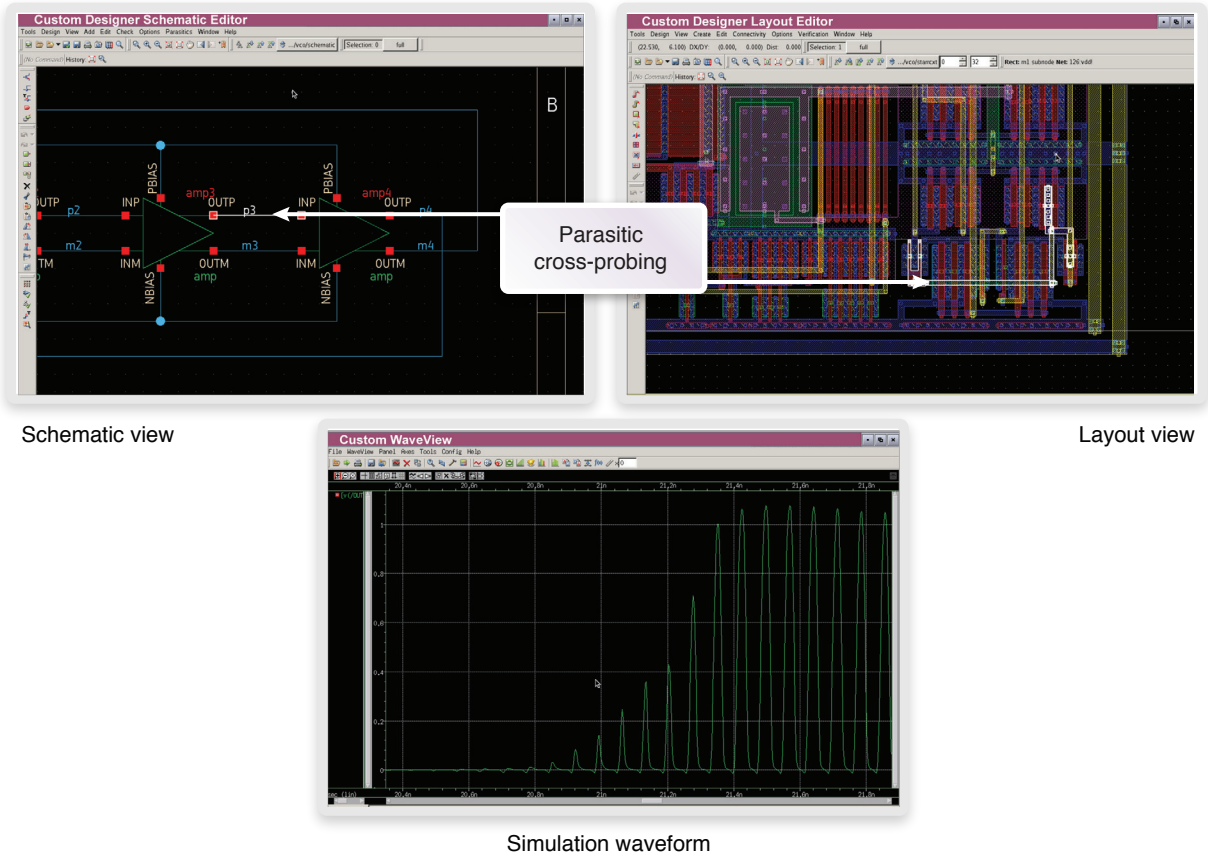


Figure 6: StarRC Custom integration with Galaxy Custom Designer enables productive cross-probing and simulation debugging

considered secondary to primary factors affecting circuit behavior, thus increasing the need for accurate modeling to mitigate the chances of silicon failure and lower yields. StarRC Custom delivers a high-accuracy solution for advanced nodes by modeling complex physical effects in smaller geometries and by accounting for every capacitive interaction in custom circuits.

At smaller process geometries, device parasitics have an increased impact on circuit behavior, especially in the case of transistor-level custom circuits. For example, gate-to-contact capacitance can have an amplified impact on device performance due to the Miller effect. Device parasitics are becoming "context-specific" at advanced nodes, that is, they are becoming more sensitive to the layout environment requiring higher levels of accuracy in extraction. StarRC Custom accurately models and extracts the device-level effects such as contact etch effect, gate-to-contact and gate-to-diffusion fringe capacitances for increased signoff accuracy (see Figure 4a, 4b).

CustomSim Circuit Simulator Integration

Post-layout simulation runtimes are increasing 2-4x with every new process generation. More accurate and efficient parasitic extraction is needed to accelerate simulation and meet tapeout schedules. StarRC Custom offers seamless integration with Synopsys' industry-leading CustomSim circuit simulator and a wide range of innovative features to boost simulation performance and capacity while preserving signoff accuracy. StarRC Custom's exclusive interface with CustomSim includes selective device parasitic extraction, active node (critical net) extraction, post-layout acceleration with isomorphic hierarchical back-annotation and optimized power network extraction (TARGET_PWRA) for faster in-design rail analysis (see Figure 5). The integration between the two tools enables over 10x simulation performance speedup for custom IC and memory designs.

Custom AMS Design Platform Integration

StarRC Custom is integrated with Synopsys' Galaxy Custom Designer mixed-signal implementation system and with Cadence's Virtuoso Analog Design Environment (ADE) for custom AMS and custom digital designs. StarRC Custom and Galaxy Custom Designer offer users the unique benefits of an OpenAccess interface combined with the ease-of-use of

the familiar Synopsys implementation environment using a common data flow. StarRC Custom provides full probing capabilities to probe parasitics within the parasitic view or within the matching schematic view (see Figure 6). The parasitic prober allows users to interactively observe point-to-point resistance, total net capacitance, net-to-net coupling capacitance and cross-probing between schematic and parasitic views. It also provides the ability to output probed parasitics to an ASCII report file, and to annotate parasitic view total capacitance values to an associated schematic view.

Other Key Features

Process Modeling

- Litho-aware extraction
- Via etch modeling
- Advanced OPC effect modeling
- Low K dielectric damage modeling
- Microloading effect (bottom thickness variation)
- Width- and spacing-dependent thickness variation
- Density-based thickness variation
- Multiple density-based variation
- Width and spacing dependent RPSQ variation
- RPSQ variation as function of silicon width Nonlinear RPSQ variation
- Trapezoidal polygon support
- Copper interconnect, local interconnect modeling
- Low-K dielectric, silicon on insulator (SOI) modeling
- Conformal dielectric process support
- Support of Air Gap
- Via cap extraction
- Layer ETCH
- Temperature-dependent resistance modeling for conducting layers and vias
- Support of background dielectric
- Nonlinear via resistance modeling
- 45-degree routing support
- Support of multiple inter-layer and intra-layer dielectric
- Support for co-vertical conductors
- Support for non-planarized metal

Productivity and Ease-of-use

- Multicore / distributed processing
- Multi-temperature-corner extraction
- Flexible parasitic reduction
- Transparent simulation setup
- License queuing
- User-control reduction of parasitic netlists
- Multiple reduction modes for different applications

Specifications

File Format Support

- StarRC Custom supports the following industry-standard formats and interfaces:
- Layout data in: GDSII, IC Validator, Hercules, Calibre
- Output formats: DSPF, SPICE, SPEF

System Requirements

- DRAM: 512MB, recommend 1GB
- Swap Space: 512MB, recommend 2GB
- Installation disk space: 250MB baseline plus 250MB per platform
- Design disk space depends on the circuit size, recommended minimum 500MB

Platform/OS

- IBM RS/6000 AIX (64)
- SPARC Solaris (32)
- SPARC Solaris (64)
- x86 Solaris (32)
- x86 Solaris (64)
- x86 Red Hat Enterprise (32)
- x86 Red Hat Enterprise (64)
- x86 SUSE Enterprise (32)
- x86 SUSE Enterprise (64)

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