STAR Hierarchical System Solution

ASIL D READY
Functional Safety
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Highlights

- Hierarchical test accelerates SoC testing
- Automated test integration and validation of digital, analog and mixed-signal IP/cores on SoC increases design and DFT productivity
- Flexible IP/core test scheduling optimizes test time and power
- Automated porting of IP/core patterns to SoC level enables re-use of test patterns
- Optimized hierarchical IEEE 1500 network reduces area and signal routes
- Efficient on-chip eFUSE programming for IP calibration/trimming
- ATE-based and interactive access to IP debug test modes enables faster production ramp
- ISO 26262 certified to meet the safety requirements of the most stringent designs targeting ASIL D

Overview

The DesignWare® STAR Hierarchical System is an automated hierarchical test solution for efficiently testing system-on-chips (SoCs) or designs using multiple IP/cores, including analog/ mixed-signal IP, digital logic cores and interface IP. The STAR Hierarchical System significantly reduces test integration time by automatically creating a hierarchical IEEE 1500 network to access and control all IP/cores at the SoC level, and increases test quality of results (QoR), including optimizing test time and power through flexible test scheduling of IP and cores. With support for IEEE 1687, STAR Hierarchical System enables standardized test and control access to complex interface IPs for efficient silicon debug and diagnostics, and allows silicon debug and diagnostics by enabling IP debug test modes from the SoC level. The system's highly automated design-for-test (DFT) implementation and hierarchical IP- and core-level test enables engineering teams to cut their test integration time to a matter of days and bring their designs to market faster with lower design and test costs.

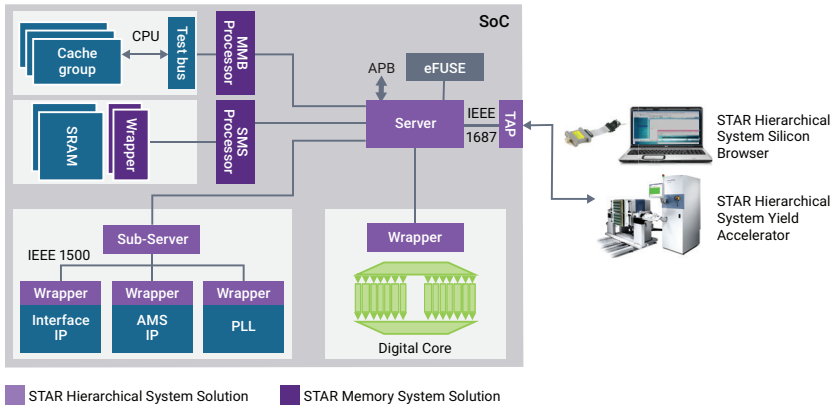

Figure 1: DesignWare STAR Hierarchical System Solution

SoC designers and silicon aggregators targeting automotive, IoT, enterprise, and consumer applications licensed STAR Hierarchical System with the added flexibility of consulting services for hierarchical test planning, generation, insertion, and verification for logic, analog, mixed-signal, and PHY IP blocks.

The STAR Hierarchical System Solution consists of:

- Configurable hierarchical test RTL IP
- STAR Hierarchical System Design Acceleration (DA) scripts: Automates the planning, generation, insertion and verification of hierarchical RTL IP
- STAR Yield Accelerator for automated pattern porting and generation of

tester-ready patterns in WGL/STIL/SVF and post-silicon failure diagnostics

- STAR Silicon Browser for interactive silicon debug of IP using a personal computer or workstation

Hierarchical Architecture

The STAR Hierarchical System creates user-configurable and broadly adopted IEEE 1500 interfaces in the RTL for each IP/core and integrates the interfaces with a top-level control module or server while maintaining a standard interface at every design hierarchy.

IP Test Integration

The STAR Hierarchical System uses an IP/core view, which includes the I/O and test information, for creating IEEE 1500 interfaces, shown as wrappers in Figure 1. The STAR Hierarchical System can automatically create an IP view for any analog/mixed-signal IP, digital logic core or interface IP. To reduce the signal routes and congestion, the STAR Hierarchical System allows wrapped IP/cores to be integrated in a daisy-chain or ring configuration. Additionally, the STAR Hierarchical System automatically creates verification testbenches, timing constraints and configuration files to enable faster design closure.

Re-Use IP Patterns

The STAR Hierarchical System utilizes the IEEE 1500 network to port IP test patterns to the SoC level, eliminating the need to regenerate patterns and reducing test development time. The STAR Hierarchical System automatically ports the serial access patterns to the SoC level.

Flexible Test Scheduling

The STAR Hierarchical System provides flexibility to schedule individual IP and cores for parallel or serial testing to optimize test time and power consumption. The server manages hierarchical test access and control of the IP and can selectively enable IP to be tested in parallel. This flexible test scheduling capability can significantly reduce test time and test cost, especially for designs with limited I/Os.

eFUSE Programming

The STAR Hierarchical System helps improve SoC yield by enabling eFUSE programming through the server for calibration and trimming of analog/mixed-signal IP. The server collects the signature needed for calibration and trimming and programs it to the eFUSEs.

Tester Patterns and Diagnostics

The STAR Hierarchical System creates tester-ready vectors in WIGL or STIL or 1687 based ICL/PDL or other common formats for the IP patterns ported to the SoC level, and provides fault analysis and root-cause failure guidance based on silicon test results. The STAR Hierarchical System leverages IP debug test modes and enables diagnostics control and access from the SoC level. The STAR Hierarchical System is compliant with the proposed IEEE 1687 standard, which allows re-use of SoC DFT instruments for board-level or system-level test and debug.

Silicon Bring-Up and Debug

The STAR Hierarchical System utilizes a test access port (TAP) to interactively communicate with the hierarchical IEEE 1500 network of the chip for post-silicon bring-up, system debug, diagnosis and characterization of IP. It enables post-silicon dignostics to be run from the engineer's desktop, without the need for expensive automatic test equipment.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.

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