STAR Memory System Solution

Highlights

- Complete memory test, repair and diagnostics solution supporting embedded SRAM, register files, CPU and GPU caches, CAM, multi ports, embedded flash, MRAM as well as external memory such as DDR/LPDDR
- Increased design productivity with hierarchical architecture and automated system-on-chip (SoC) integration and verification
- High-quality test to provide full memory defect coverage with minimum test time
- High yield with efficient on-chip repair across multiple operating corners
- Superior diagnostics with physical failed bitmaps and XY coordinate identification to quickly determine root cause of failures
- Increased field reliability with STAR Memory System Compiler for Error Correcting Codes' (ECC) multi-bit transient error correction
- ISO 26262 certified to meet the safety requirements of high reliability designs targeting up to and including the most stringent ASIL D standard
- Supports Internet of Things (IoT) applications with the industry's first commercial built-in self-test (BIST) solution for embedded flash and embedded MRAM (eMRAM)

The Synopsys Self-Test and Repair (STAR) Memory System™ is a comprehensive, integrated test, repair and diagnostics solution that supports repairable or nonrepairable embedded memories across any foundry, process node or memory IP vendor. Silicon-proven in over a billion chips on a range of process nodes, the STAR Memory System is a cost-effective solution for improving test quality and repair of manufacturing faults found in advanced technologies like FinFET. The STAR Memory System's highly automated design implementation and diagnostic flow enables SoC designers to achieve quick design closure and significantly improve time-to-market and time-to-yield in volume production.

The STAR Memory System has been certified for the ISO 26262 automotive functional safety standard by SGS-TUV Saar GmbH, an independent accredited assessor. In addition, the test and repair support for e-flash and embedded MRAM (eMRAM) enables the STAR Memory System to be used in IoT applications.

SoC designers, silicon aggregators, and leading foundries targeting automotive, IoT, enterprise, and consumer applications license STAR Memory System with the added flexibility of consulting services for memory BIST planning, generation, insertion, and verification.

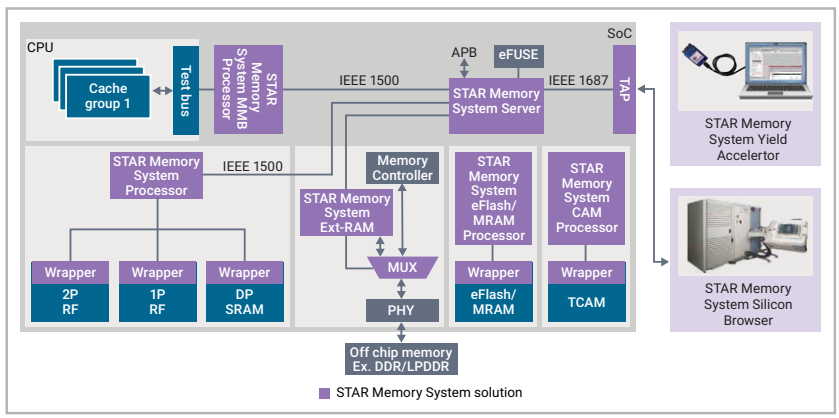

Figure 1: Synopsys STAR Memory System Solution

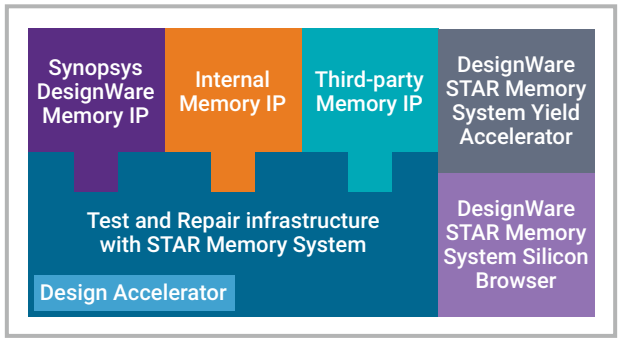

Figure 2: The Synopsys STAR Memory System helps save millions of dollars in recovered silicon, reduces test costs, and shortens time-to-volume

The STAR Memory System Solution Consists of:

- Synthesizable test and repair register transfer level (RTL) IP
- STAR Memory System Design Acceleration (DA) scripts: Automates the planning, generation, insertion, and verification of test and repair RTL IP
- STAR Memory System Yield Accelerator: Automates the generation of tester ready patterns in WGL/STIL/SVF, test algorithm programmability and post silicon failure diagnostics and fault classification
- STAR Memory System Silicon Browser: Provides interactive silicon debug of memory using a personal computer or workstation
- STAR Memory System ECC: Automatically generates ECC Verilog code, testbenches and scripts for single-port and multiport SRAM memories
- STAR Memory System ext-RAM: Offers a high-coverage, cost-effective test with optional Post Package Repair (PPR) and diagnostics solution for external memories such as DDR, LPDDR and HBM via JTAG, either during production or in-field test
- STAR Memory System CAM: Supports specialty content addressable memory (CAM) such as binary, ternary and XYCAMs with support for common CAM capabilities
- STAR Memory System eMRAM: Optimizes manufacturing yield for eMRAM technology with inclusion of NVM specific test algorithms and support for trimming in addition to test, repair and diagnosis

Flexible, Open System

To provide STAR Memory System access to all memory developers, Synopsys offers a specialized memory description language called MASIS. The MASIS language, together with a MASIS compiler, simplifies and automates the process of creating and verifying memory views used by the STAR Memory System. By providing an open interface to the STAR Memory System, Synopsys extends the value of the system to all users regardless of whether or not they elect to use Synopsys memories (Figure 2).

High-Performance Core Support

The STAR Memory System allows at-speed test and repair of high-performance processor cores by using a preconfigured test bus, which provides access to the memories inside the core in test mode. The STAR Memory System uses this shared Multi-Memory Bus (MMB) to test memories and add memory test and repair logic outside the IP core to avoid any impact on processor core performance (Figure 1).

Test Algorithm Programmability

The STAR Memory System provides full test algorithm programmability. The STAR Memory System processor includes a BIST module to execute test algorithms. The default test algorithms in the BIST module can be replaced with new algorithms in the RTL or in silicon, and the user can program either their own custom algorithms or select from the comprehensive library of algorithms provided in the STAR Memory System.

Tester Patterns and Diagnostics

The STAR Memory System Yield Accelerator addresses the need to identify, analyze, isolate and classify memory faults as designs are readied for transition from first silicon to volume manufacturing rapidly, cost-effectively and accurately. Leveraging the infrastructure of the STAR Memory System, the Yield Accelerator automatically generates vectors for test equipment and provides fault analysis and root-cause failure guidance based on silicon test results. Using this feature, test and product engineers can rapidly analyze failures manifested in embedded memories and inspect the physical location and class of each fault to determine the root cause without involving the IP vendor or SoC designer.

On-Chip Self-Repair

Unlike complex external repair flows, the STAR Memory System's on-chip repair is fully automated. A built-in self-diagnosis module determines the location of any memory defect and provides error logging by scanning out failure data for silicon debug. When testing memories with redundancies that have failures, a built-in repair and redundancy allocation module identifies available redundant elements and determines the best possible redundancy configuration.

Integrated Test and Repair with Synopsys Embedded Memories

By hardening the timing-critical test and repair logic within the memory hard macro, the Synopsys STAR Memory System provides unique integration with Synopsys Embedded Memory Compilers. Optimal placement of the timing-critical test and repair logic near the memory allows faster design closure, higher performance, better area and reduced power.

Silicon Bring-up and Characterization

The STAR Memory System Silicon Browser has advanced automation capabilities to interactively communicate through a JTAG port with the STAR Memory System's infrastructure in a chip for post-silicon bring-up, system debug, diagnosis and characterization of embedded memories. The unique features of the Silicon Browser allow full extraction of memory contents, multi-corner and multi-voltage characterization, precise physical failure localization, defect classification and redundancy utilization analysis, all from an engineer's desktop, and without the need for expensive automatic test equipment.

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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