Synopsys RedHawk-SC Electrothermal

Multiphysics Platform for Multi-Die 2.5D/3D-IC Systems: Thermal, Power, Structural, and Signal Integrity Signoff

Overview

Next-generation semiconductor products tailored for networking, AI and high-performance computing (HPC) applications increasingly rely on multi-die technologies to drive system density, speed, and improved yield. The range of 2.5D/3D-IC technologies available today incorporate multiple die, an interposer, a package, and a printed circuit board (PCB) connected by millions to billions of tiny connections. Design and verification of these advanced silicon assemblies is challenging and requires a system technology co-optimization (STCO) approach to address the increased coupling effects across multiple physics. Synopsys RedHawk-SC Electrothermal™ is an innovative and comprehensive chip-centric multiphysics simulation platform for 2.5D/3D-IC prototyping, analysis and signoff. It provides simulation engines to address all relevant physics domains and ensure thermal, power, signal, and structural integrity in a system context.

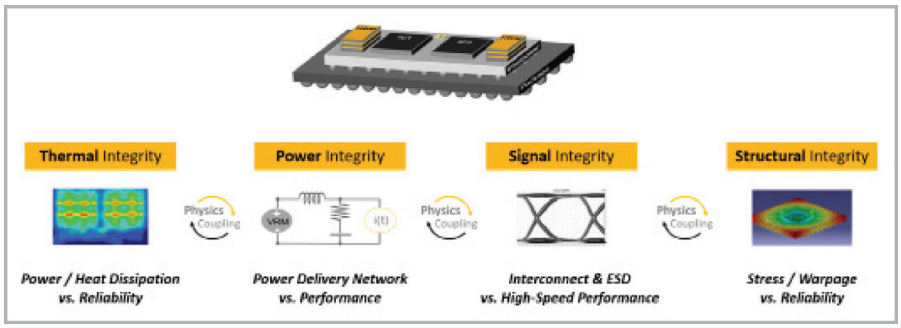

Figure 1: Multiphysics analysis of multi-die assemblies with Synopsys RedHawk-SC Electrothermal

Highlights

Synopsys RedHawk-SC Electrothermal is a chip-centric multiphysics simulation platform based on industry-standard Synopsys golden solvers and offers multiphysics analysis and signoff for 2.5D/3D-IC multi-die systems. It features a unified cockpit to orchestrate the high-capacity electrical model and thermal model for the entire chip-package-system with multiple die, interposer, package, and PCB interconnected by billions of micro bumps, through-silicon vias (TSVs), and hybrid bonding pins. With full support for TSMC's 3Dblox format for input collaterals, RedHawk-SC Electrothermal tool provides prototyping components for 3D-IC feasibility analysis and layout components for power and thermal design signoff. It can be used by chip and package designers to concurrently address the issues arising from monolithic single chips as well as multiple die with an interposer in a 3DIC design. These

include thermal-induced mechanical stress, multi-die voltage-drop, multi-die electrostatic discharge (ESD) verification, electromagnetic interference (EMI), and power-noise-induced signal integrity problems. RedHawk-SC Electrothermal is foundry certified for 2.5D/3D-IC power integrity, signal integrity and thermal integrity signoff. Foundry certifications include TSMC CoWoS/InFO/SoIC technology, Samsung X-cube, and Intel EMIB packaging with backside power distribution technology.

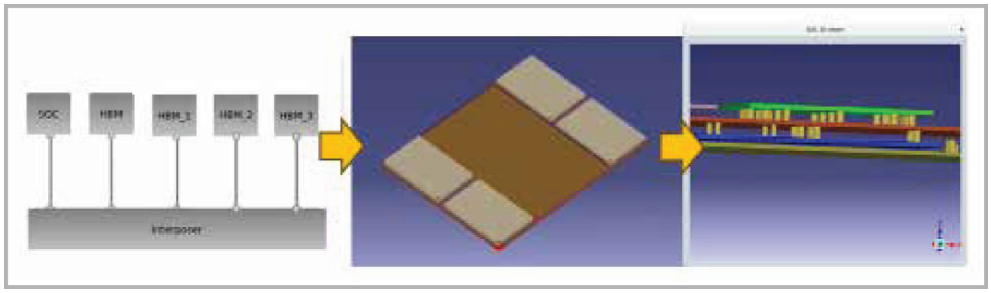

Figure 2: RedHawk-SC Electrothermal modeling of 3D multi-die assemblies with interposer and packaging substrate

3D-IC Component Modeling, Extraction and Assembly

Synopsys RedHawk-SC Electrothermal features a 2.5D/3D-IC component assembly capability to connect multiple die, interposer, and package into a system-level physical model. The platform is powered by cloud-native Synopsys Seascape platform and patented machine learning algorithms to support high-capacity electrothermal analysis for early design exploration, post-layout design verification and design signoff of the chip-package-system. At the design feasibility stage, all components can be represented by an electrical or thermal model, facilitating fast prototyping for power and thermal integrity analysis. Similarly, at the design and signoff stage the layout files with parasitic and thermal information can be extracted for all components to perform accurate and high-capacity power or thermal signoff. RedHawk-SC Electrothermal supports the open-standard TSMC 3Dblox language for interoperability with other 3DIC electronic design automation (EDA) tools such as Synopsys 3DIC Compiler™. To enable 3D-IC heterogeneous system co-simulation, Synopsys CPM™ (chip power model), CTM™ (chip thermal model) and CSM™ (chip signal model) are reduced order models (ROM) that are used to build a hierarchical model for accurate and rapid power and thermal integrity simulation. Millions to billions of micro-bump or hybrid bond connections can be assembled through a smart pin-grouping algorithm to facilitate 3D-IC IR drop, electromigration, ESD simulation flow with Synopsys reliability tools.

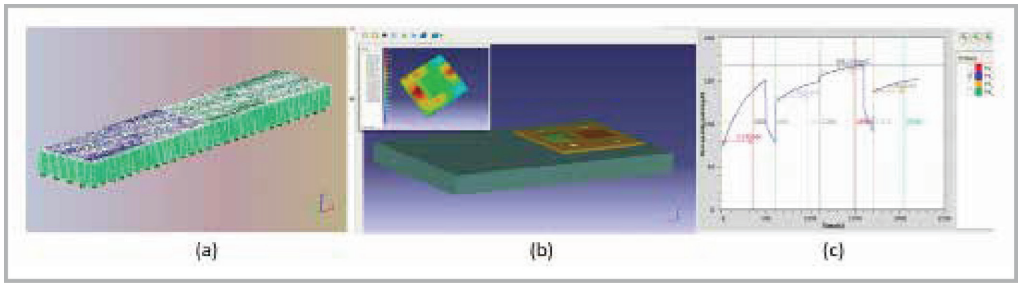

Figure 3: Signal integrity analysis by RedHawk-SC Electrothermal showing interposer PDN extraction (a), impedance frequency profile (b), and eye diagram with power noise (c)

2.5D/3D-IC Thermal Integrity Analysis and Signoff

RedHawk-SC Electrothermal has incorporated the industry gold-standard mechanical solver from Ansys Mechanical™ to build the 2.5D/3D-IC structural model for thermal conduction simulation. It employs an adaptive finite element method (FEM) to perform submicrometer high-resolution thermal simulation of advanced process technologies. It supports anisotropic thermal properties which are important to simulate accurate thermal conduction of the latest backside power distribution technologies. Static thermal analysis considers the temperature-dependent power of active dies to calculate the Tmax location of the entire 3D-IC system layer stackup. Fast transient thermal analysis is used to design thermal management and thermal throttling. This is done with either a power-state table or emulator-generated long patterns.

Interposer/3D-IC Power and Signal Integrity Analysis and Signoff

RedHawk-SC Electrothermal is well integrated with Synopsys HFSS-IC™ for modeling signal integrity challenges due to electromagnetic coupling/interference between high-speed signals running long distances on interposers. It also captures the impacts of system power noise. A powerful user GUI enables a rich set of signal integrity-power integrity (SIPI) models such for input/outputs (IO), interconnect, decoupling capacitors, and signal channels. This provides a comprehensive set of eye-diagram analysis and JEDEC-compatible check capabilities.

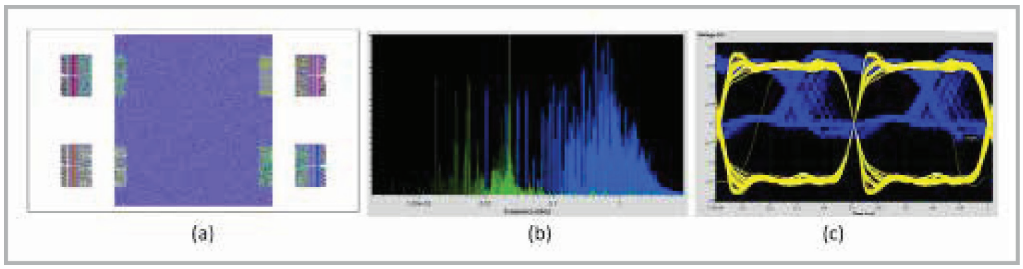

Figure 4: Multi-die multiphysics results for power flow (a), static thermal (b), and transient thermal (c)

Multiphysics and Multi-scale Simulation Capability

RedHawk-SC Electrothermal interfaces with several Synopsys signoff tools to deliver accurate multiphysics coverage that is essential to avoid under- or over-design. Thermal analysis provides the junction temperature profile between the die and the package to RedHawk-SC for thermal-aware electromigration analysis needed for individual die signoff. In addition, RedHawk-SC Electrothermal can take the die pad current profiles from RedHawk-SC to perform a package and PCB electrothermal co-simulation that models the Joule heating effect of currents in the wires. Any thermal analysis of a 2.5D/3D-IC module requires boundary conditions set by thermal convection and thermal conduction by heat sinks. RedHawk-SC Electrothermal thermal analysis obtains these boundary conditions, called system heat transfer coefficients (HTCs), from Ansys AEDT Icepak™ to deliver silicon-correlated results. Temperature variation across an assembly will inevitably result in stress and warpage in the components. RedHawk-SC Electrothermal integrates the Ansys Mechanical™ solver for structural integrity simulation and identify design weaknesses in the 2.5D/3D-IC system caused by thermal-induced stress. Finally, by linking with Ansys optiSLang™, users can perform parametric sensitivity analysis of block floorplanning, power source assignment, thermal boundary conditions, signal net geometry, and other design variables to discover the optimal Multiphysics design configuration for early-stage or signoff co-optimization.

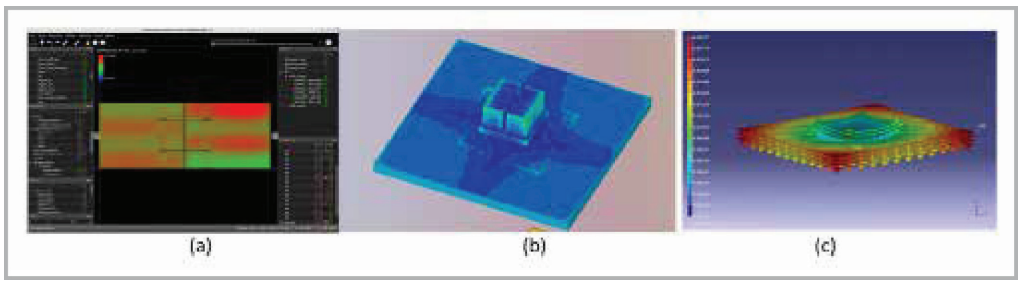

Figure 5: RedHawk-SC Electrothermal multiphysics analysis results for thermal-aware electromigration signoff (a), thermal integrity with system boundary conditions (b), and thermal-induced stress and displacement (c)