PrimeSim

Unified Workflow of Next Generation Technologies to Accelerate Design of Hyper-converged ICs

Overview

Continuous technology scaling and shift towards multi-die and heterogenous design integrations have given rise to hyper-converged designs with a significant increase in scale and system complexity. Advanced technology nodes present increased parasitics and process variations, and large heterogeneous system-in-package designs demand complex multi-dimensional analysis and improved QoR, time-to-results, and cost-of-results. Addressing these complex needs requires a holistic and cohesive approach to design and verification and disparate tools and flows will prove to be inadequate.

PrimeSim provides a unified workflow of next-generation simulation technologies to accelerate the design and signoff of hyper-converged designs. PrimeWave, a newly architected design verification environment, is integrated with PrimeSim to deliver a seamless simulation experience around all PrimeSim simulation engines.

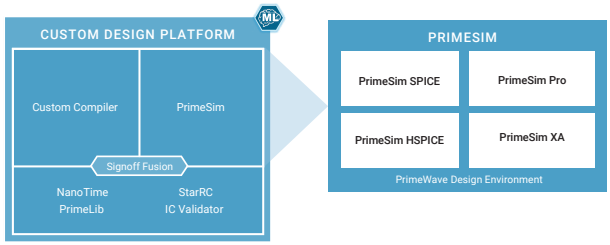

Figure 1: PrimeSim Solution

Key Benefits

- Unified workflow around PrimeSim HSPICE, PrimeSim SPICE, PrimeSim Pro, and PrimeSim XA
- PrimeSim SPICE and PrimeSim Pro with advanced SPICE and FastSPICE architectures and breakthrough GPU acceleration technology deliver up to 10X faster runtimes with signoff accuracy
- PrimeSim HSPICE delivers gold-standard signoff accuracy for foundation IP and signal integrity
- PrimeSim XA delivers the industry's highest performance for SRAM and mixed-signal verification
- PrimeWave Design Environment provides an open and consistent design environment across all simulation engines with comprehensive analysis and improved productivity and ease of use

A Unified Workflow to Accelerate Design of Hyper-converged ICs

The PrimeSim unified workflow enables users to seamlessly deploy industry-leading SPICE and FastSPICE simulation engines to address the full spectrum of design verification needs. Users can effortlessly step through library characterization and signal integrity analysis using PrimeSim HSPICE, advanced analog and RF analysis using PrimeSim SPICE, mixed-mode and chip-level analysis using PrimeSim Pro and PrimeSim XA across memory, analog, RF, and custom digital designs.

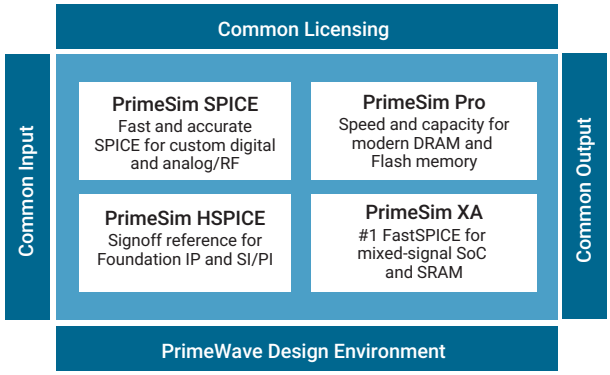

Figure 2: PrimeSim Unified Workflow

Faster Runtime with Signoff Accuracy

The PrimeSim next-generation SPICE and FastSPICE engines—PrimeSim SPICE and PrimeSim Pro—feature advanced architectures and data models, and breakthrough GPU acceleration technology to deliver up to 10X faster runtime with signoff accuracy, Advanced circuit partitioning, accurate load models, and a new GPU solver enable breakthrough performance accelerating verification of large post-layout analog, RF, SerDes, and full chip DRAM and Flash designs.

Open and Consistent Design Environment

PrimeSim unified workflow is complemented by PrimeWave Design Environment which provides a consistent design environment with comprehensive setup, analysis, and visualization capabilities. Featuring a powerful TCL-based scripting capability and a high-capacity waveform viewer, PrimeWave Design Environment delivers a rich simulation experience and superior ease of use.

Foundry-certified, ISO 26262 Compliant, and Cloud Ready

- The PrimeSim simulation engines—PrimeSim HSPICE, PrimeSim SPICE, PrimeSim Pro, and PrimeSim XA—are certified with leading foundries such as TSMC and Samsung Foundry on advanced nodes
- PrimeSim technologies are part of the ISO 26262 TCL1 certified Synopsys Custom Design tool chain and thus can be reliably used to verify functional safety for ASIL-D applications
- The PrimeSim simulation engines are also cloud-ready with enablement and optimization for leading public cloud platforms

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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