PrimeShield

Improving design robustness and silicon lifecycle efficiency

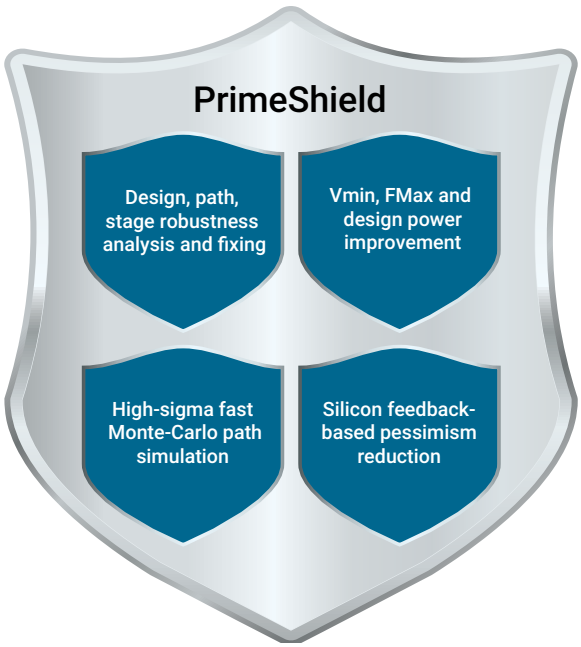
Overview

PrimeShield provides design robustness analysis and fixing at advanced nodes and enables designers to effectively reduce design power and boost frequency. PrimeShield helps designers:

- Improve design robustness in face of escalating process and voltage variability
- Minimize over-pessimism, over-margin and over-design
- Maximize silicon lifecycle management efficiencies

PrimeShield can rapidly identify and drive optimization of bottlenecks at the stage, path and design level that are sensitive to variations such as supply voltage drops or manufacturing variability. The patented fast statistical methods and breakthrough machine learning technology delivers 100X-1000X faster design robustness analysis and optimization than existing solutions. It is scalable to volume production system-on-chips (SoCs) with billions of transistors, while using industry standard inputs for immediate deployment.

PrimeShield can also intelligently leverage silicon data and measurements, enabling designers to shift-left design robustness optimization to pre-silicon design phases. It can enable silicon-feedback based timing model prediction for design optimization and silicon-correlated design. It provides improved silicon analytics and flow for silicon debug and production ramp.



PrimeShield Capabilities

The PrimeShield innovative fast statistical engine uniquely leverages the core engines of the industry's gold-standard PrimeTime® signoff and HSPICE® simulation tools. It overcomes the turnaround time challenges that previously prohibited full statistical design variation analysis with machine learning technologies, enabling analysis and optimization for every design of any size.

Accelerated by machine learning technology, the PrimeShield solution performs fast Monte Carlo statistical simulation on critical timing paths with HSPICE accuracy within minutes, versus days or weeks required by full statistical simulations. Its patented design variation analysis with statistical correlation modeling enables analysis and optimization on large-scale SoCs with billions of cells, an analysis previously feasible only for a few dozen cells.

The addition of robustness as a fourth design quality metric, now PPAR (power, performance, area, and robustness), enables Fusion Design Platform™ to deliver silicon designs that are faster, lower power, more robust and more cost effective.

Improved Design Robustness

Variation Robustness, Design Variation Analysis, and Fast Monte Carlo Path Simulation identify bottleneck cells, improve overall design variation robustness, and enables use of Monte Carlo path simulation for production waiver flow.

High-Performance Design

PrimeShield helps reduce the over-margins for process variation, voltage variation and FEOL/BEOL mis-tracking to boost the design FMax frequency with increased accuracy and predictability.

Low-Power Design

Voltage Robustness and Vmin Analysis identify IR timing bottlenecks from all the cells and compute voltage slack for each critical or near critical path to improve design resilience to IR drop and enables power saving (by pushing down VDD).

Automotive/High-Volume Design

High-sigma, high-reliability design with >1000x fast Monte Carlo speedup to deliver HSPICE accuracy for mission critical applications in hours, and minimize timing-induced failures, ensuring low DPPM (Defective Parts Per Million).

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