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Accelerating Innovation

Power Compiler

Power Optimization in Design Compiler

Overview

Power Compiler™ automatically minimizes power consumption at the RTL and gate level, and enables concurrent timing, area, power and test optimizations within the Design Compiler® synthesis solution. It performs advanced clock gating and low power placement to reduce dynamic power consumption, and performs leakage optimization to reduce standby power. Power Compiler along with Design Compiler Graphical utilizes concurrent multi-corner multi-mode (MCMM) optimization to reduce iterations and provide faster time-to-results. With power intent defined by the standardized IEEE 1801 Unified Power Format (UPF), designers can use Power Compiler to implement advanced low power techniques such as multi-voltage, power gating, and state retention.

While advances in process technology bring unprecedented performance to electronic products, they pose difficult power dissipation and distribution problems. These problems must be addressed because consumers demand both high performance and long battery life in medical devices, smartphones, tablet computers, and other mobile appliances, as well as energy efficiency in traditional "plugged-in" devices. Power Compiler enables complete and comprehensive power-aware synthesis within Design Compiler (Figure 1). By applying Power Compiler's power reduction techniques during synthesis, designers can perform concurrent timing, area, power and test optimization.

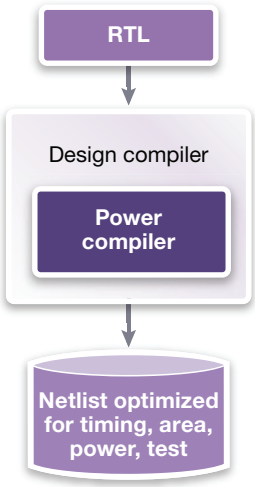

Figure 1: Complete, comprehensive power synthesis within Design Compiler

Key Benefits

- Advanced clock gating and low power placement for lower dynamic power
- Leakage power optimization for lower standby power
- Concurrent multi-corner multi-mode based optimization for faster time-to-results
- Automated implementation of UPF-driven advanced low power techniques

Advanced Clock Gating

Power Compiler reduces dynamic power consumption by gating the clocks of synchronous load-enable register banks instead of circulating the outputs back to the inputs when the load-enable conditions are invalid (Figure 2). The operations are performed automatically during the design elaboration phase without requiring any changes to the RTL source, enabling fast and easy trade-off analysis and maintaining technology-independent RTL source. Power Compiler's clock gating can also be performed at the gate level and can complement manual clock gating. The tool supports several advanced clock gating techniques, including self-gating, multi-stage, latency-driven, activity-driven (using SAIF files) and user-instantiated clock gating.

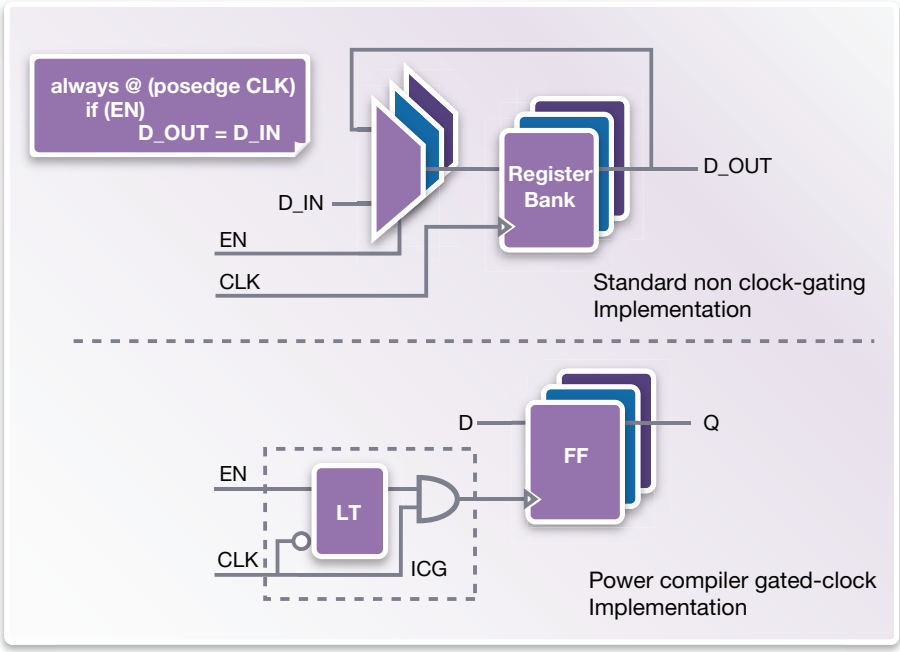

Figure 2: Power Compiler performs automatic clock gating to reduce dynamic power consumption.

Low Power Placement

In addition to clock gating, Power Compiler along with Design Compiler Graphical, performs power-aware placement, This capability utilizes the same technology as IC Compiler to minimize net length on signals with high switching activity, in order to minimize dynamic power consumption.

Leakage Power Optimization

Power Compiler reduces leakage power using multi-voltage threshold based optimization, or by the designer's specifying a maximum percentage of low-voltage threshold cells to be used in a design. Power Compiler measures the trade-offs between positive timing slacks, area and power, and delivers the lower power-consuming design that meets the timing constraints.

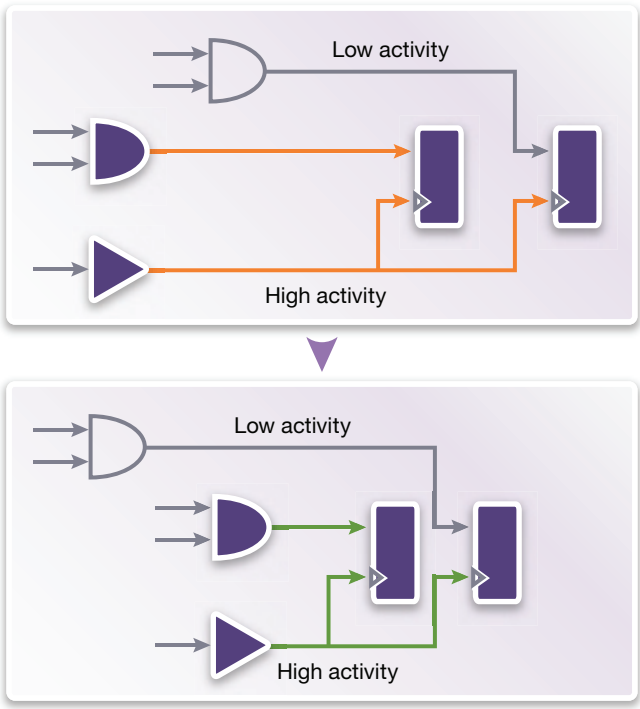

Figure 3: Power-aware placement minimizes capacitance on high activity nets

Concurrent Multi-Corner Multi-Mode Based Optimization

Concurrent MCMM optimization is essential for fast turnaround time when implementing designs that can operate in many modes such as test mode, low-power active mode, stand-by mode, etc. One of the primary benefits of MCMM is the ability to achieve optimal leakage results without performing either leakage

power optimization on the same corner as timing optimization or successive leakage-timing optimizations (using different corners for worst-case timing and worst-case leakage).

MCMM optimization in Design Compiler Graphical and Power Compiler takes all of the different process corners into account to provide the best leakage results with minimal impact on performance. The ability to concurrently optimize for multiple modes and corners enables rapid design convergence through fewer design iterations. Used with UPF power intent specification, MCMM serves as the key enabling technology for performing dynamic voltage and frequency scaling (DVFS).

Automated Implementation of Advanced Low Power Techniques

Early definition of power intent in the design flow enables downstream tasks in the process to be automated and driven by a consistent power specification. Power intent includes the specification of multiple voltage supplies, power domains, power shutdown modes, isolation, voltage level shifting and state retention behavior. Power intent written in the IEEE 1801 Unified Power Format (UPF) is used systematically throughout the design process to describe the design power intent, and is captured as a companion file to the RTL or gate level design. This power intent automates the implementation of the advanced low power capabilities employed.

Power Compiler takes UPF input and automatically inserts power management cells such as isolation, level-shifter, retention register, power gating and always-on cells as needed based on the power domain, strategy and state definitions. It also supports a "golden UPF" flow that preserves original power intent across the entire design flow.

Netlist Formats and Interfaces

Power Compiler is seamlessly integrated with the Synopsys synthesis design flow and shares the same GUI, commands, constraints and libraries as the Design Compiler and IC Compiler® tools. It supports all popular industry standard formats and platforms.

Circuit Netlist:

- Verilog, SystemVerilog, VHDL

Interfaces:

- SDF, PDEF, SDC

Platforms:

- IBM AIX (32-/64-bit)
- Redhat Linux (32-/64-bit)
- Sun Solaris (32-/64-bit)

Summary

Power Compiler delivers complete and comprehensive power synthesis within Design Compiler, including advanced clock gating for dynamic power savings, leakage power optimization for lower standby power and concurrent MCMM of leakage and timing corners. Power Compiler also supports automated implementation of low power methodologies using UPF.

For more information on Synopsys' Advanced Low Power Solution, visit www.synopsys.com/lowpower.

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