SYNOPSYS®

DATASHEET

NanoTime Transistor-level STA

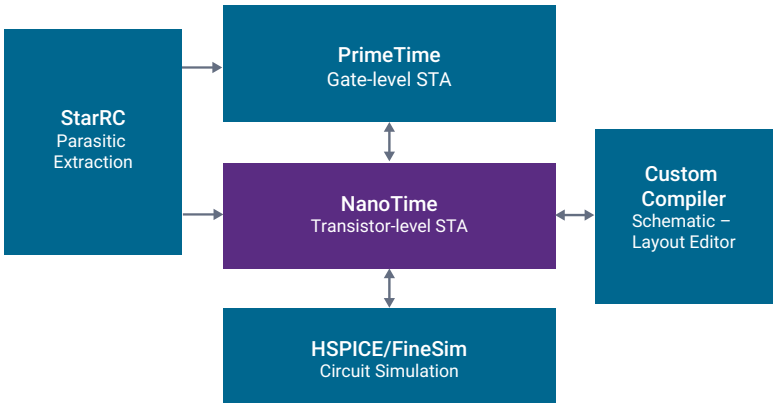
Custom Digital, Memory and Mixed Signal Signoff Analysis

NanoTime is the key foundry certified, golden signoff solution for transistor level design

Overview

Timing verification is essential to make sure your design will function and perform as expected when it is manufactured in silicon. To ensure complete coverage of all timing paths, static timing analysis should be used to compliment dynamic simulation. For advanced process technologies such as FinFet, the impact of process variation and signal integrity needs to be accounted for. Additionally, functional failures caused by glitch noise should be found and fixed before final sign-off.

NanoTime is the key foundry certified, golden signoff solution for transistor level design. It performs transistor level static timing, signal integrity and process variation analysis for complex custom designs such as CPU datapaths, register files, embedded memories and complex intellectual property (IP) blocks. NanoTime when used to in conjunction with PrimeTime® enables full-chip signoff of mixed gate- and transistor-level designs.



Transistor-level Static Timing Analysis

Often optimizing chip performance, area and functionality requires using full-custom design for key sub-components. For these critical blocks, verification using transistor-level dynamic simulation can be very time consuming and is often incomplete. Failing to analyze all critical paths in a design can result in either slower than expected chip performance or failing silicon particularly due to hold time violations. NanoTime traces all possible paths in the design, checking for timing violations at the intersection of clock and data to ensure setup and hold time requirements are met. The path reports from NanoTime can be used to drive design optimization and to find and fix potential silicon failures before tapeout.

Transistor-level Signal Integrity Analysis

For advanced nodes, analyzing the impact of signal integrity (SI) on timing is essential as crosstalk from adjacent signals can change path delays by as much as +/-25%. NanoTime identifies potential victim and aggressor nets and accounts for both the speeding up and slowing down of signals based on their worst-case switching alignment. In addition, crosstalk can induce noise glitches that can cause functional failures if they propagate and disturb stored logic states in latches or flip-flops. By finding these failures with NanoTime costly silicon re-spins can be avoided.

Transistor-level Process Variation Analysis

For advanced designs how to manage the impact of process variation on timing is essential to improving yield. Simply derating delays by constant on chip variation (OCV) factors across the design is too pessimistic for most paths but not pessimistic enough for some others. Understanding how process variation impacts each component within the context of a path (Parametric On-Chip Variation (POCV)) enables a much more realistic analysis which designers can use to optimize their design. NanoTime calculates the impact of process variation on the delay and slew of each path stage and statistically accumulates the impact over the complete path. NanoTime also supports global variation analysis using a method known as Path Based Slack Adjustment (PBSA) that considers common clock path segments when calculating timing slack.

Simultaneous Switching Signals

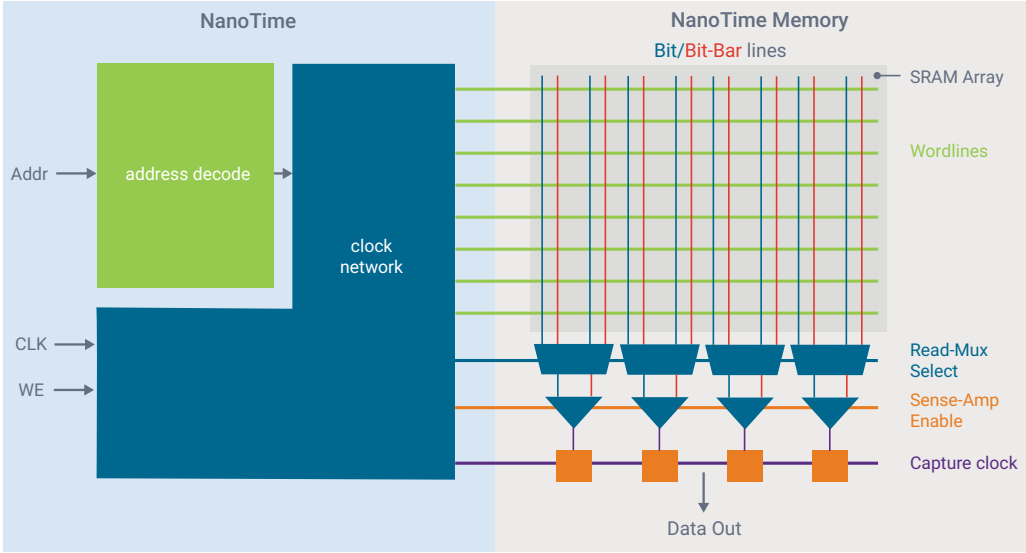
Static timing analysis typically assumes each signal will switch independently. However sometimes signals are designed to switch simultaneously to boost performance or inadvertently coincide. NanoTime can analyze the impact on timing from multiple simultaneous signal transitions. This includes support for full swing differential circuits and the impact of multiple input switching (MIS). For both differential analysis and MIS, NanoTime can iterate to model the skew between the various switching inputs to ensure the most accurate result. These iterations will also incorporate SI delay effects ensuring changes in signal arrival times (timing windows) are accounted for.

Block Characterization Enables Full Chip Timing Signoff

Transistor- and gate-level static timing analysis need to work seamlessly together to achieve full chip timing verification. NanoTime can analyze and characterize transistor-level blocks and generate an extracted timing model (ETM) for inclusion in full-chip timing by PrimeTime. The ETM model supports standard Liberty format timing models including composite current source (CCS) models for timing, composite current source models for noise (CCSN) and Liberty Variation Format (LVF) for process variation. To achieve higher productivity, NanoTime supports many of the same commands as PrimeTime including Synopsys Design Constraints (SDC). NanoTime also supports mixed level netlists where portions of the design can be modeled using a Liberty model. This can be used, for example, to black-box analog components such as current mirrors, that are not well suited to static analysis.

Embedded Memory Design Analysis

Embedded memory designs present unique challenges for transistor-level static timing analysis due to the large size of the memory array and the analog nature of the sense-amp. The NanoTime Memory Option addresses these challenges by identifying the memory array (bit cells, word line, sense-amp and mux circuitry) and using a direct interface to distributed dynamic simulation (HSPICE® or FineSim®) to determine the worst-case paths through the array. The results of the dynamic simulation are then seamlessly integrated and reported along with NanoTime's built-in analysis of the remaining circuitry (address decode etc.). The NanoTime Memory Option also supports automated timing checks unique to memories to prevent design errors due to race conditions.



Key Features

- Concurrent transistor-level timing, signal integrity, and process variation analysis of complex custom designs such as datapaths, register files, embedded memory and analog mixed signal blocks
- Foundry certified including TSMC, Samsung, UMC, Global Foundries and ST
- Accuracy within 3%, 3ps of HSPICE
- Multi-million transistor capacity including back-annotation of parasitics (SPF, SPEF) from StarRC® or third-party extraction
- Block characterization (.lib) including LVF, CCS timing and CCS noise models
- NanoTime Memory Option includes array simulation and race condition checks
- Mixed-level design analysis (transistors, cells and black-box (.lib)) support
- Supports both Multi-input switching (MIS) and full swing differential signal analysis
- Dynamic clock tree analysis with HSPICE and/or FineSim circuit simulators
- Common interface with PrimeTime (Tcl commands, SDC, path reporting)
- Noise glitch functional failure analysis
- ISO 26262 Certified