SYNOPSYS®

DATASHEET

IC Compiler

Place and Route System

Comprehensively addresses the time-to-market, power, performance and area requirements

Overview

The IC Compiler™ place and route system is a single, convergent, chip-level physical implementation tool. It includes flat and hierarchical design planning, placement, clock tree synthesis, routing and optimization, manufacturability, and low-power capabilities that enable on schedule delivery of advanced designs. For Synopsys' latest place-and-route system refer to IC Compiler II.

Benefits

IC Compiler delivers all the technology required to realize both mainstream and advanced designs at multiple process nodes. IC Compiler shares technology with and correlates to Design Compiler Graphical, the PrimeTime® SI solution and the StarRC™ parasitic extraction tool to ensure a fast and monotonic path from design implementation to final signoff. Additionally, IC Compiler In-Design technology enables early physical verification and fixing using IC Validator technology and accurate foundry runsets.

- IC Compiler is a complete place-and-route system for established and emerging process technology node designs
- IC Compiler hierarchical design technology enables powerful design planning and early chip level exploration/analysis features to handle large, complex designs
- IC Compiler delivers smaller die size with predictable design closure to reduce the cost of design
- IC Compiler with Zroute digital router technology utilizes advanced routing algorithms, concurrent manufacturability optimizations and multi-threading, to improve manufacturability and deliver faster turn-around-time
- IC Compiler In-Design technology seamlessly integrates the IC Validator signoff DRC and metal fill solution allowing designers to mitigate manufacturing compliance challenges in the implementation stage for faster signoff closure
- IC Compiler is part of the Synopsys Design Platform and is tightly correlated to the industry-standard signoff solutions—PrimeTime SI and StarRC with value links to Design Compiler Graphical

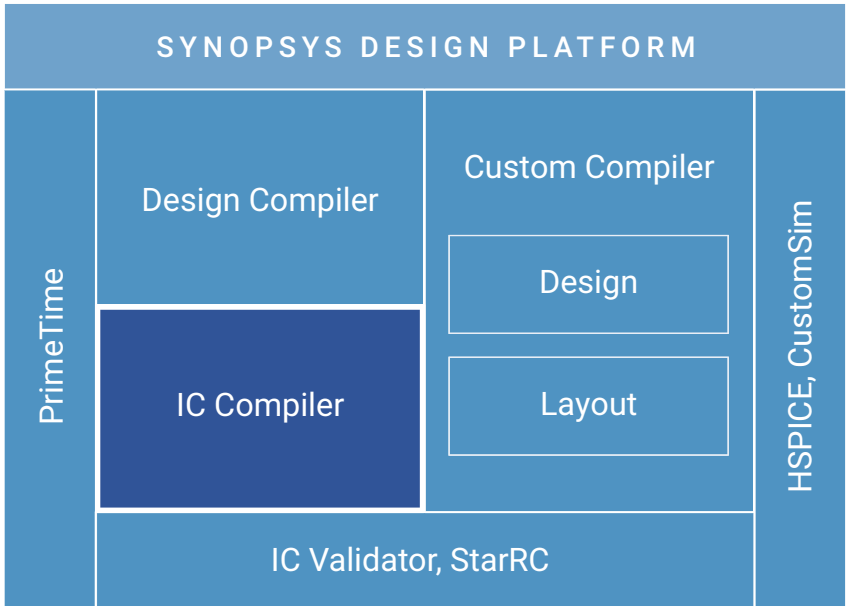

Figure 1: Synopsys Design Platform

IC Compiler benefits the physical designer in three key categories: Quality of Results (QoR), Turnaround Time (TAT), and Cost of Design.

Quality of Results

Innovative multicorner multimode (MCMM) and multivoltage (MV) technologies in IC Compiler digital implementation system delivers improved QoR, measured in terms of the complete cost vector.

- **CCD:** Concurrent clock and data (CCD) optimization technology delivers optimal QOR for advanced designs and complex clocking architectures. CCD technology is a key enabler for high-speed processors and SoCs
- **Arm cores:** IC Compiler delivers high-performance Arm core tapeouts. Performance, power and area (PPA) targets are met with a wide arsenal of key technologies, such as: clock mesh, CCD, physical datapath, hierarchical design planning, multi-power domains, route-based optimizations, MCMM, Zroute, UPF and minimum physical impact (MPI) ECO

Turnaround Time

IC Compiler provides the fastest path to results. This is achieved using best in-class engines, multicore support, powerful design planning capabilities, and complete, faster convergence throughout the design stages, culminating in unrivalled signoff accuracy.

- **Data flow analysis:** Data flow analysis (DFA) during design planning enables fast and optimum block placement in large block dominated designs. Data flow visibility allows the designer to minimize path lengths through block array design and orientation, speed up design planning, and improve timing budget quality
- **MPI-ECO:** Minimum physical impact (MPI) technology reduces tapeout delays due to late stage ECOs. MCMM and multivoltage-aware MPI leverages PrimeTime signoff ECO guidance to place ECO cells with minimum disturbance to the existing layout and to re-use as much of the existing route segments as possible, resulting in faster, more accurate ECOs and better turn-around time
- **Zroute:** Zroute technology digital router technology in IC Compiler utilizes advanced digital routing algorithms and multi-threading capability to take full advantage of the multi-core compute platforms delivering much faster turn-around time. The modern Zroute architecture incorporates state-of-the-art routing technology, such as native soft rules to enable litho-friendly routing and avoid manufacturing problems. Employing concurrent manufacturability optimization techniques, Zroute simultaneously considers the impact of manufacturing rules, redundant vias, timing and other design goals to deliver the highest QoR along with improved manufacturability

Cost of Design

IC Compiler allows designers to utilize a variety of techniques to meet timing, power, area, routability, and yield goals. This reduces the cost of design and increases predictability.

- **MCMM:** Concurrent MCMM-aware placement, clock tree synthesis, routing, and optimization transformations dramatically reduce TAT for large, complex chips with multiple numbers of modes and corners. Intelligent optimization is driven by timing, area, power, signal integrity, routability and yield cost factors that are measured concurrently across all scenarios. IC Compiler's MCMM solution eliminates the ping-pong effects seen at later stages of the design flow
- **Double patterning and beyond:** Double patterning (DPT) or multiple-patterning starting at 20nm and below designs requires at least two masks to correctly manufacture integrated circuits with current lithography equipment. Additionally, IC Compiler and In-Design physical verification with IC Validator offers an accelerated multi-patterning closure solution
- **FinFET support:** Complete FinFET support is another benefit of the early co-development collaboration between Synopsys and the leading foundries. IC Compiler fully supports FinFET use through all physical design stages

IC Compiler is a complete physical implementation solution. For detailed information regarding a specific technology need, please contact your local Synopsys account teæam or visit www.synopsys.com.