SYNOPSYS®

DATASHEET

Fusion Compiler

Predictable RTL-to-GDSII implementation system delivers up to 20% better quality of results

Overview

Fusion Compiler™ is the next generation RTL-to-GDSII implementation system architected to address the complexities of advanced process node design and deliver up to 20% improved quality-of-results (QoR) while reducing time-to-results (TTR) by 2X. Fusion Compiler is built on a compact, single data model that allows seamless sharing of Fusion Technology across the RTL-to-GDSII flow to enable hyper-convergent design closure. Fusion Compiler was built from the ground-up using best-in-class RTL synthesis, place-and-route, and signoff technologies for designing state-of-the-art SoCs that deliver unmatched power, performance, and area (PPA), QoR, and fast design convergence. Fusion Compiler's integrated cockpit (Figure 1) provides a comprehensive platform for design including RTL physical synthesis, design planning, placement, clock tree synthesis (CTS), advanced routing, physical synthesis-based optimization, chip finishing, signoff quality analysis and ECO optimization.

Key Benefits

- Comprehensive RTL-to-GDSII design system delivers up to 20% better PPA and 2X TTR
- Fusion data model architecture for unmatched capacity, scalability, and productivity
- Unified physical synthesis optimizations for best QoR
- Common placement and 2D legalization engines for fast DRC convergence and design closure
- Accurate congestion estimation and prediction using route-driven estimate for overall convergence
- Complete flow power optimization including unique power-driven re-synthesis and knee-based optimization
- Physically-aware synthesis and advanced CTS to drive highest frequencies
- Leading foundry process certified FinFET and multi-patterning aware design
- Signoff timing, parasitic extraction, and power analysis eliminate design iterations
- Advanced area recovery algorithm from synthesis to post-route for best utilization
- Pervasive parallelization with multi-threaded and distributed processing technologies for maximum throughput

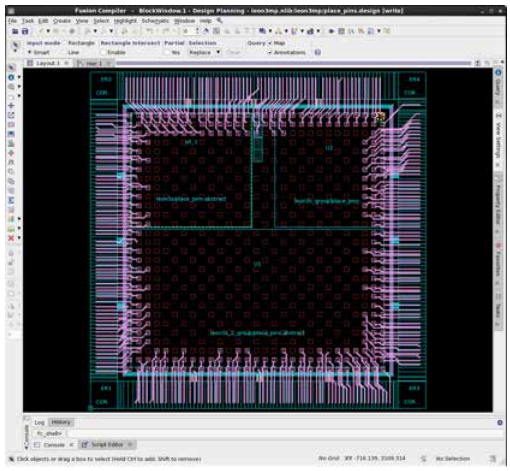

Figure 1: Integrated Fusion Compiler RTL-to-GDSII cockpit

Fusion Data Model

The Fusion Compiler single data model contains both logical and physical information to enable sharing of library, data, constraints, and design intent throughout the implementation flow. The advanced data model is architected to support ultra-large designs with the smallest possible memory footprint. The key innovation of Fusion Compiler is synthesis and implementation tools access to each others technology, including sharing of optimization engines between the two domains. Fusion Compiler integrates all synthesis, place-and-route and signoff engines on a single data model and eliminates data transfer delivering fastest design closure with highest throughput.

2X Faster Time to Results

Fusion Compiler enables the fastest turnaround time from RTL-to-GDSII by blurring the boundary between synthesis and physical implementation with a unified physical synthesis optimization flow. The scalable architecture handles the complexities of advanced node designs and its native hierarchical infrastructure can handle hundreds of millions of instances. The robust system and complete feature set supports all design styles, producing the most optimal floorplan configurations in the shortest time. Parallelization technologies, multi-threading and distributed processing of key engines throughout the flow utilize hardware resources effectively for fast design convergence and rapid design closure. The core implementation engines including synthesis, placer, optimizer, CTS, and router have been revamped to significantly speed-up design implementation. Signoff quality engines throughout Fusion Compiler eliminates the need for adding excessive design margins and eliminates late stage convergence issues.

Up to 20% Better Power, Performance, and Area

Fusion Compiler offers unique and innovative solutions that spans both RTL physical synthesis and place-and-route domains including interleaved floorplanning and synthesis, physically-aware data path representation, logic re-synthesis during physical implementation and a common Unified Physical Synthesis (UPS) optimization that delivers up to 20% better QoR. UPS is the nerve center and fundamental backbone for all optimization capabilities within Fusion Compiler that unifies the best technology from next generation synthesis and place-and-route optimization engines for faster convergence (Figure 2). UPS offers advanced features such as layer-aware optimization, macro skewing, advanced 2D legalizer, route-driven estimate (RDE) for modeling congestion, concurrent clock and data (CCD), multi-bit banking and de-banking, total power centric optimization, auto non-default rule (NDR), and via ladder support for advanced nodes.

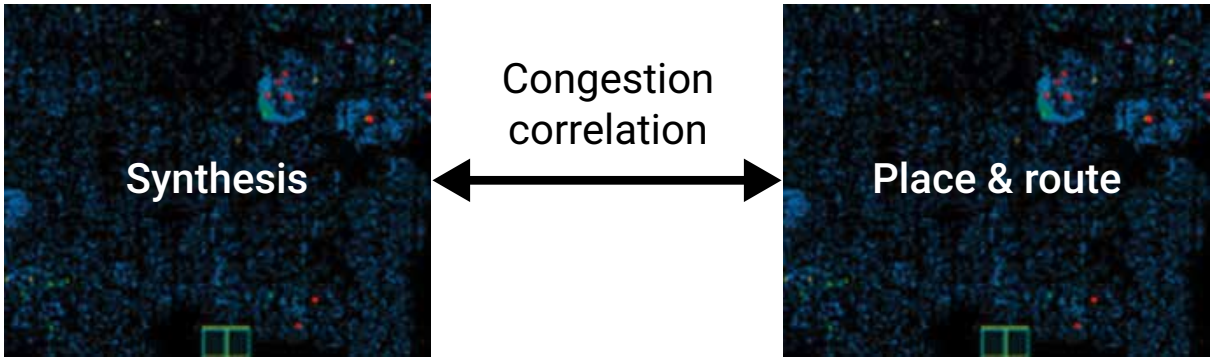

Figure 2: Unmatched correlation and QoR with unified physical synthesis

Advanced Node Enablement

Fusion Compiler provides a comprehensive multi-patterning and FinFET-aware implementation solution that is certified by leading foundries for all advanced process nodes. During synthesis UPS advanced legalizer handles inbound cells and regular standard cells as well as multi-bit registers while considering the trade-offs to meet timing and area constraints. The placement engine is engineered to support the fin grid (Figure 3), spacing rules for implants, continuous diffusion, variable threshold cell spacing rules and cross row rules to minimize multi-patterning violations. The routing engine supports complex routing rules including cut-metal aware routing, preferred grid extension, via pillars, and intelligent multi-patterning avoidance and fixing.

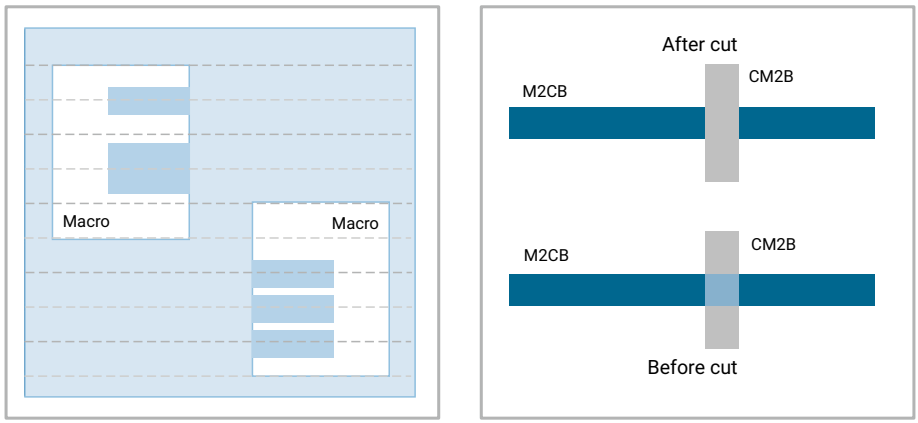

Figure 3: Fusion Compiler fin grid and cut-metal support