SYNOPSYS®

DATASHEET

Design Compiler NXT

2X faster runtime, superior quality-of-results, and a new cloud-ready distributed processing engine

Overview

Building on the industry-standard Design Compiler® Graphical to continue delivering innovative synthesis technology, Design Compiler NXT delivers 2X faster runtime, superior quality-of-results (QoR), and a new cloud-ready distributed processing (DP) engine. The technology links from Design Compiler Graphical into IC Compiler™ II are further strengthened to tighten timing, parasitic resistance and capacitance correlation between synthesis and place-and-route. Design Compiler NXT synthesis technology is enabled for next-generation process node technologies including below 5nm.

Key Benefits

- Builds on the benefits of Design Compiler Graphical, by enabling a new, advanced feature set to improve designer productivity and yield better QoR at the most advanced design nodes
- Plug-and-play, user interface (UI) and script compatible with Design Compiler Graphical
- 2X faster runtime, with improved multi-threading technology for better scalability up to eight CPUs
- 5% better QoR for dynamic power, through advanced optimizations and concurrent clock and data (CCD) technology
- New cloud-ready distributed processing, using intelligent workload partitioning without QoR trade-off
- Next-generation process node support, including below 5nm
- Enhanced physical guidance to IC Compiler II, with improved RC and timing correlation
- Shares a common library and block abstract models with IC Compiler II, and retains support for the MilkyWay™ library format

2X Faster Runtime

Significantly faster runtime accelerates design closure for even the most technologically advanced integrated circuit (IC) designs. Inside Design Compiler NXT, core engine speed-ups improve runtime across a wide variety of customer designs, and achieve better scalability up to eight cores by using a new smart multi-threading technology to further improve runtime across all synthesis optimization stages. In addition, the new DP engine uses intelligent workload partitioning, where the partitions are sent to different machines for optimization but operate with the full physical and logical context of the design. This approach enables further speed-ups which are particularly beneficial for the larger design sizes found at advanced nodes without QoR trade-off.

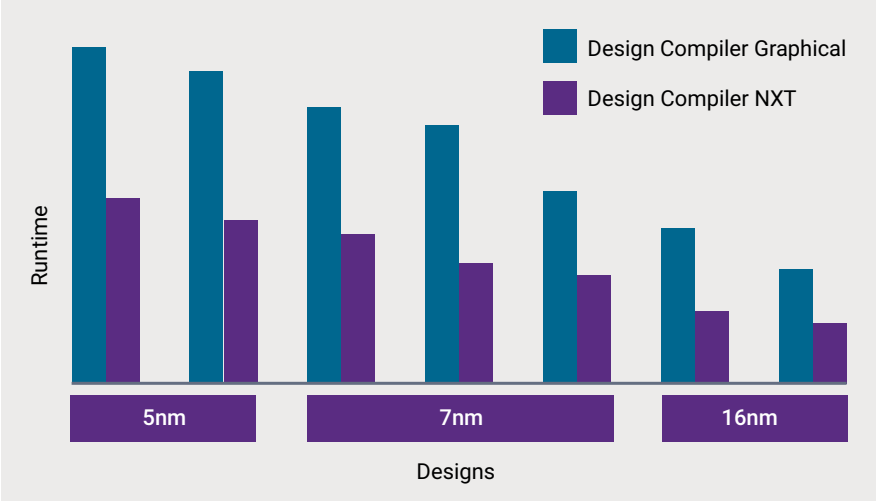

Figure 1: Design Compiler NXT runtime improvement

5% Better Quality-of-Results

Optimizations yield 5% dynamic power savings. New techniques are introduced for mapping, restructuring, rewiring, and other operations to reduce dynamic power without degrading timing, area, or congestion. Deployment of CCD technology from IC Compiler II improves timing and power recovery through dynamic management of skew.

Enablement Across all Leading-Edge Processes

Design Compiler NXT is the leader in synthesis for advanced nodes down to and below 5nm. Leadership at advanced nodes is maintained with continued support for via pillars, pattern must join, auto non-default rule (NDR), pin access awareness, variant-aware libraries, layer-aware optimization, and other requirements. New synthesis capabilities are being developed to meet foundry requirements and customer expectations of the performance, power and area (PPA) benefits from the next production process node in development.

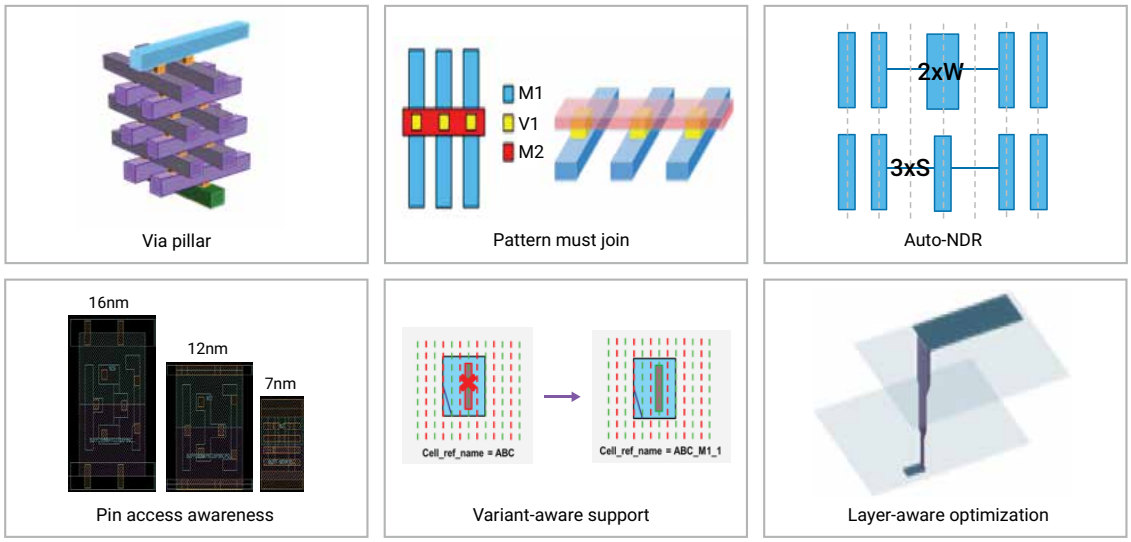

Figure 2: Advanced process node support

Enhanced Physical Guidance to IC Compiler II

With designs becoming more complex at smaller geometries, RTL designers require even tighter correlation between synthesis and layout results. To achieve the most efficient RTL-to-GDS flow, parasitic estimations of net topology are aligned between Design Compiler NXT and IC Compiler II, such as unit RC modeling and via estimations, while also considering local density during the parasitic calculations. The correlation between synthesis and place-and-route is further improved by using high-accuracy timing models for path-by-path and endpoint-by-endpoint calculations.

Common Library and Block Abstract Models

Design Compiler NXT users benefit from sharing a common library and block abstract models with IC Compiler II because they can use the same libraries for both synthesis and place-and-route. If library models are updated as a design is being developed, then there is a reduced risk that libraries will get out of synchronization between synthesis, place-and-route, and physically-aware signoff-driven ECO. At the same time, Design Compiler NXT continues to support Milkyway for full backwards compatibility.

Building on the Capabilities of Design Compiler Graphical

- Design Compiler NXT is plug-and-play, UI and script compatible with Design Compiler Graphical
- Cross-probing between RTL and design views such as schematic, timing reports and physical views for faster debugging
- Early physical visualization and debugging identifies layout issues prior to physical implementation
- Floorplan exploration for faster design convergence to an optimal floorplan
- Accurate pre- and post-synthesis congestion prediction and congestion-driven optimization eases routing
- Gate-to-gate optimization for smaller area on new or legacy designs while maintaining timing QoR
- Concurrent multi-corner, multi-mode (MCMM) synthesis

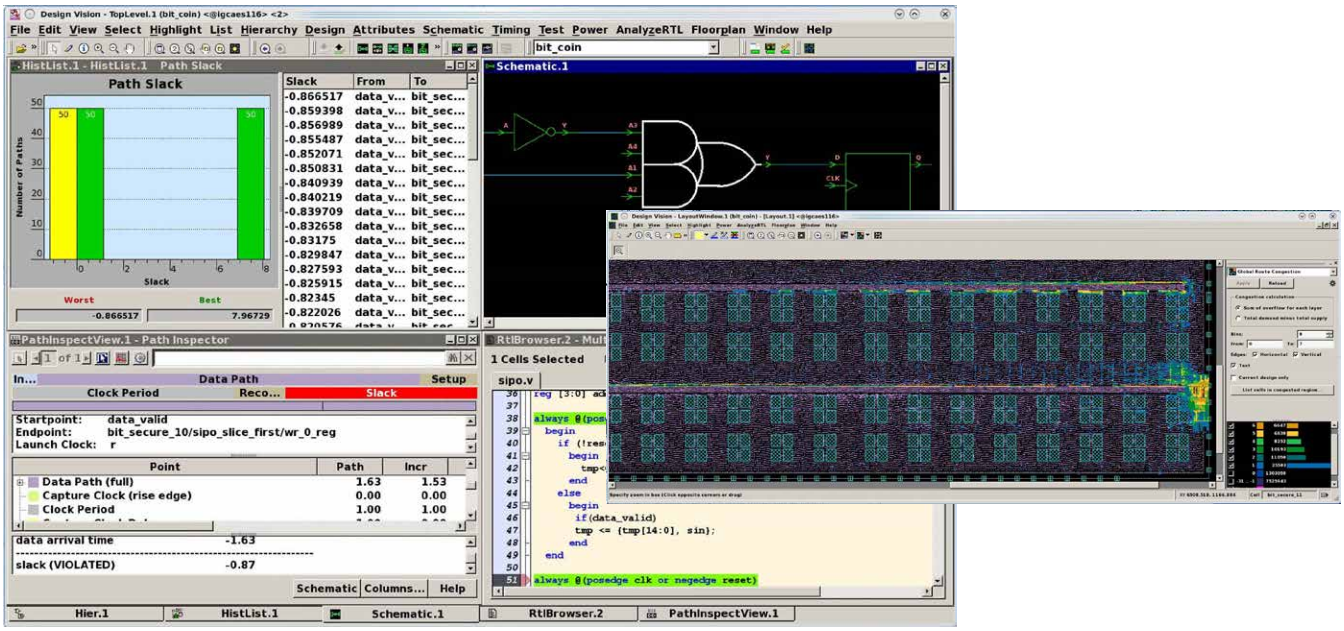

Figure 3: Cross-probing between RTL, schematic, timing, and layout views

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