Custom Compiler

Visually-assisted Automation

Cut FinFET layout tasks from days to hours

Overview

Custom Compiler™ is Synopsys' full-custom solution that features the pioneering visually-assisted automation flow to speed up common design tasks, reduce iterations and enable reuse. Tuned for rapid implementation of FinFET-based mixed-signal circuits, Custom Compiler is ideally suited to tackle tough advanced-node custom design challenges.

Introduction

Custom Compiler shortens FinFET design tasks from days to hours. Its visually-assisted automation flow leverages the graphical use model familiar to layout designers while eliminating the need to write complicated code and constraints. With Custom Compiler, routine and repetitive tasks are dealt with automatically without extra setup. The visually-assisted automation flow in Custom Compiler is based on four types of Assistants: Layout, In-Design, Template and Co-Design.

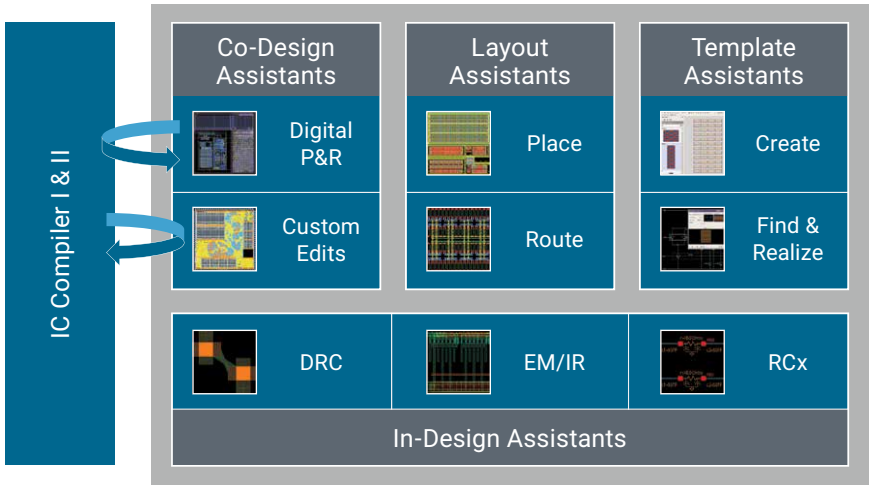

Figure 1: Custom Compiler visually-assisted automation flow

Custom Compiler Assistants

Layout Assistants speed layout with visually-guided automation of device placement and routing. The placer uses a new innovative approach to device placement. It works iteratively with the user, offering placement choices but leaving the layout designer in full control of the results —without requiring any up-front constraint entry. The router is ideal for connecting FinFET arrays or large-M factor transistors. It automatically clones connections and creates pin taps. The user simply guides the router with the mouse and it fills in the details automatically. Figure 2 shows the router connecting up

the gates of an interdigitated fully-matched differential pair. The yellow flightline shows the starting point of the route and the current cursor position. The router has automatically tapped to the pins and has cloned the routing to the devices in the rows below.

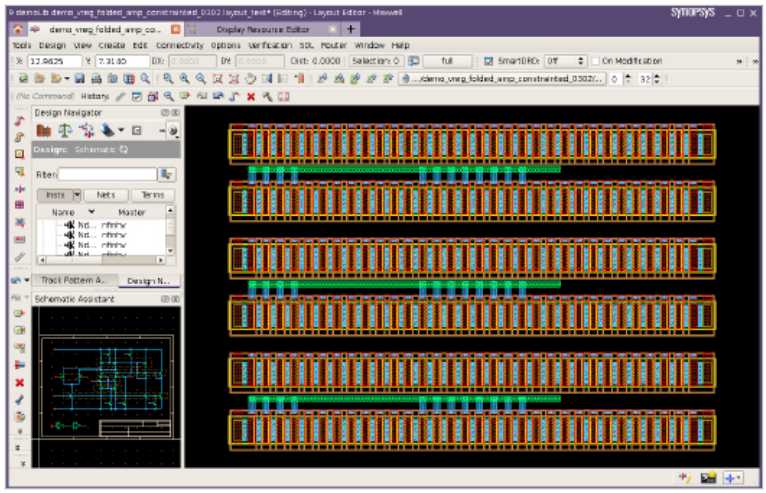

Figure 2: Interactive routing with automatic cloning and pin tapping

In-Design Assistants reduce costly design iterations by catching physical and electrical errors before signoff verification. Custom Compiler includes a built-in design rule checking (DRC) engine, which is extremely fast and can be active all the time. In addition to the DRC engine, electromigration checking (see Figure 3), and resistance and capacitance extraction are all natively implemented in Custom Compiler. Unlike other "electrically-aware" tools, Custom Compiler's extraction is based on Synopsys' gold-standard StarRC™ engine.

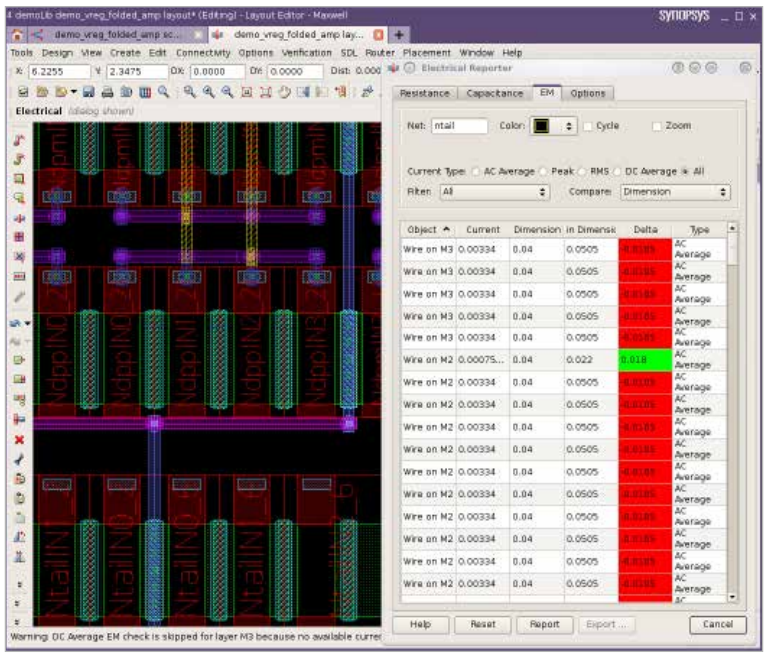

Figure 3: Electromigration checking

Template Assistants help designers reuse existing know-how by making it easy to apply previous layout decisions to new designs. Template Assistants actually learn from the work done with the Layout Assistant's placer and router. They intelligently recognize circuits that are similar to ones that were already completed and enable users to apply the same placement and routing pattern as a template to the new circuits. Custom Compiler's Symbolic Editor, for example, comes pre-loaded with a set of built-in templates for commonly-used circuits, such as current mirrors, level-shifters and differential pairs. Figure 4 shows the resulting patterns that have been found for a differential pair.

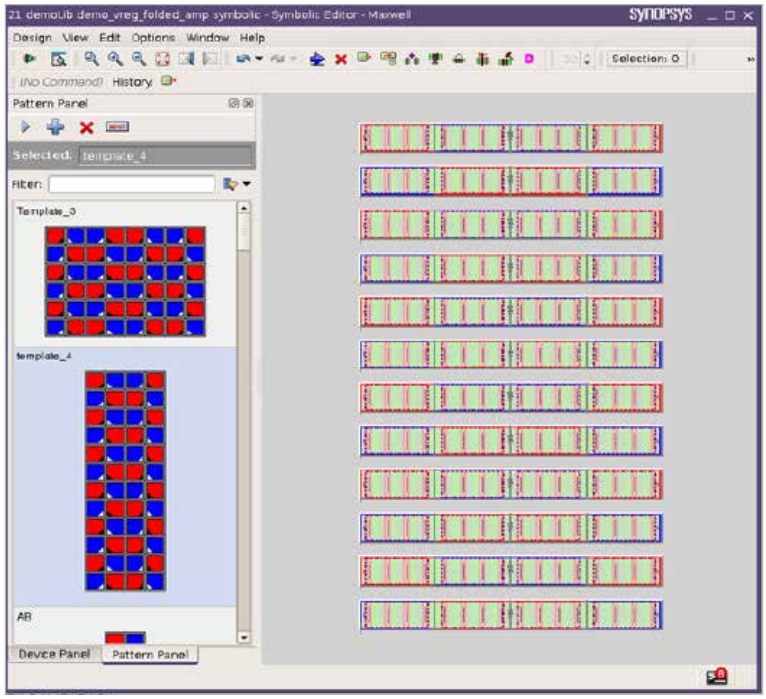

Figure 4: Example of templates for a differential pair

Co-Design Assistants combine IC Compiler™ and Custom Compiler into a unified solution for custom and digital implementation. Users can freely move back and forth between Custom Compiler and IC Compiler, using the commands of each to successively refine their designs. With the Co-Design Assistants, IC Compiler users can perform full-custom edits to their digital designs at any stage of implementation, as shown in Figure 5. Likewise, Custom Compiler users can use IC Compiler to implement digital blocks in their custom designs. The lossless, multi-roundtrip capability of the Co-Design Assistants ensures that all changes are synchronized across both the digital and custom databases.

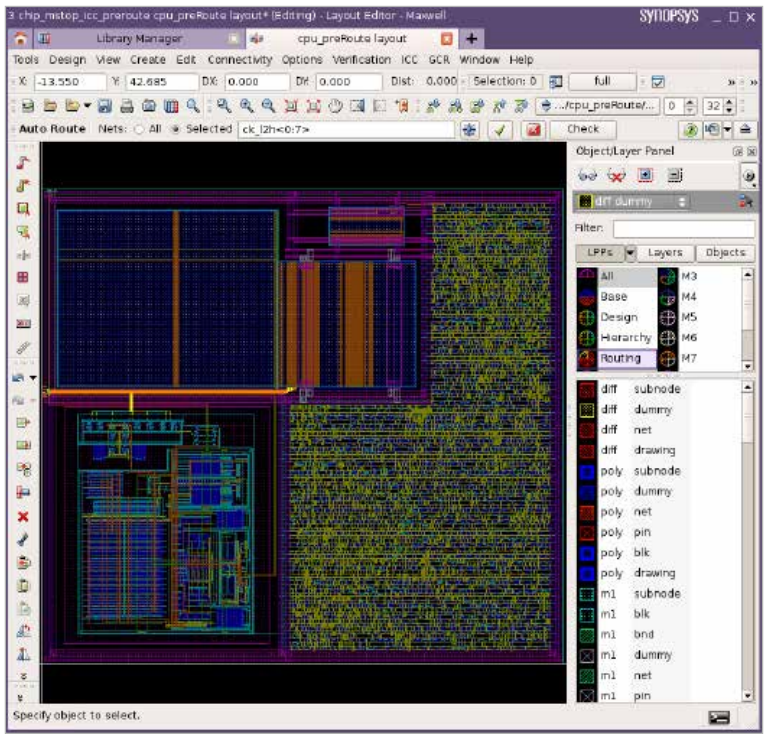

Figure 5: Full custom edits on an IC Compiler design

Custom Compiler provides an open environment and a feature-rich schematic entry and simulation environment able to handle the massive amounts of simulation data needed to ensure robust FinFET designs, coupled with a fast, highly-efficient layout editor. Custom Compiler shares the same native simulation and analysis environment that accompanies HSPICE®, FineSim® and CustomSim™.

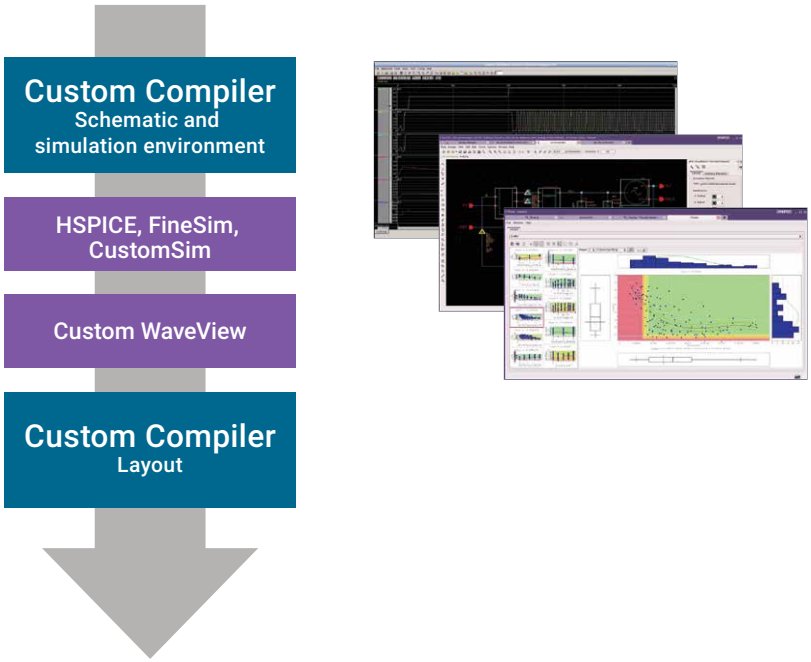

Figure 6: Simulation and analysis environment

The GUI-based environment provides a powerful user interface for analog verification. Features of the environment include advanced analyses with HSPICE, FineSim and CustomSim, multi-testbench with chaining, multi-corner and Monte Carlo simulation setup and simulation job distribution and monitoring.

Custom Compiler is based on the industry standard OpenAccess database. It features an intuitive menu structure that ensures a minimal learning curve for experienced layout engineers. It provides an open environment spanning schematic, simulation analysis and layout. Unified with Synopsys' circuit simulation, physical verification and digital implementation tools, Custom Compiler provides a comprehensive custom design solution. Custom Compiler is highly customizable with unique features that simplify the layout of complex FinFET structures. Great attention has been given to maximizing designer productivity and throughput via a unique blend of automation while still retaining the control custom designers require to optimize their circuits. To maximize tool flexibility and customization, TCL, Python and C++ are supported, any of which can be freely mixed in the same design and flow. Custom Compiler supports the iPDK standard, and foundry design kits for Custom Compiler are widely available.

For more information about Custom Compiler, visit www.customcompiler.info.