Overview
Synopsys’ unified solution for custom and cell-based design and verification provides a comprehensive, highly integrated suite of tools for advanced-node mixed-signal SoC design. This suite of tools provides a single vendor solution addressing all major aspects of SoC design. The high degree of integration and interoperability shortens time-to-tapeout and improves design quality.

Custom IC Solution Highlights
Synopsys’ unified solution (see Figure 1) for custom and cell-based design and verification includes:

- Full custom schematic and layout editing with native support for OpenAccess
- Open architecture, compliant with industry standard interoperable PDKs (iPDK)
- Unified custom and digital physical implementation
- Integrated analog simulation and analysis environment
- Industry-reference, high performance SPICE and FastSPICE simulators
- Highest performance mixed-signal simulation
- Advanced AMS regression and analysis environment
- Integrated physical (signoff) verification and parasitic extraction
- Access to world’s largest mixed-signal IP portfolio

Figure 1: Synopsys Custom Design Solution
Schematic Entry and Layout Editing
Galaxy Custom Designer® SE and LE are the next-generation choice for schematic entry and layout editing, enabling users to meet the challenges of today’s nanometer designs with little or no learning curve. Architected from the ground up with maximum productivity in mind, schematic editing and layout tasks are accomplished with fewer clicks, quicker menu access, and less pop-up menu clutter.

Custom Designer SE offers fast schematic editing. Its on-canvas parameter editing and display with dynamic connectivity, continuously maintains up-to-date design integrity for faster design, with fewer errors and less effort.

An integral component of the full-custom design system, Custom Designer LE provides block- and transistor-level layout and editing capabilities in a unified platform for both cell-based and mixed-signal custom content. Custom Designer LE enables ultra-fast layout editing with advanced P-cell support and timesaving layout automation through capabilities like intelligent multipart paths that maintain DRC correctness.

Custom Designer SE includes a complete simulation and analysis environment that combines testbenches, simulator setups, measurements, and Custom WaveView™ waveform display (see Figure 2), as well as post-simulation processing and analysis into a single environment for fast visualization of results. A single common testbench can be used for both pre- and post-layout simulation. Cross-probing and back-annotation between the simulation environment, Custom Designer SE, Custom Designer LE and extracted views lets designers quickly select and display the results that matter for quick analysis directly on the schematic or in Custom WaveView.

SmartDRD Design-Rule-Driven Layout
Built into Custom Designer, SmartDRD technology provides high-performance features for design-rule-driven (DRD) layout editing. SmartDRD technology includes:

- **DRDVisual**: concurrently checks hundreds of rules in real-time and provides error visualization in Custom Designer LE
- **DRDAssist**: enables layout designers to perform DRC-correct layout tasks at a zoomed-out “high altitude” view, greatly reducing the number of zooming-in and zooming-out iterations. DRDAssist ensures DRC correctness by keeping objects separated at the design rule distance, in-real time. DRDAssist can use multiple rule sets, such as minimum rules or recommended rules, and the rule sets can be switched on-the-fly
- **DRDAutoFix**: provides automatic correction of detected DRC violations, largely eliminating manual violation repair via polygon editing.

![Figure 2: Custom WaveView Displaying an Eye Diagram](image-url)
Custom and Mixed Signal Design Solution

Open and Extensible Environment
Based on Si2’s OpenAccess database and extensible through the industry-standard TCL scripting language, Custom Designer’s open environment allows CAD groups to quickly add new tools. Custom Designer’s open environment also includes a programmable netlister that ships with open-source code, allowing quick implementation of custom netlist formats and extracted views. The netlister supports iCDF parameters, including PEL/AEL expressions, and iCDF “simInfo” as well as netlisting.

Process Design Kits (PDKs)
Custom Designer process design kits are compliant with the industry-wide IPL Alliance that created a standard for Interoperable PDK Libraries (iPDKs). The IPL standard enables a single iPDK to be used by any OpenAccess tool without any translation. 10 leading foundries are supplying iPDKs from 28nm to 350nm, and more are becoming available. Check with Synopsys for the latest information on iPDK availability.

Accelerated SoC Implementation with IC Compiler Custom Co-Design
Synopsys’ IC Compiler digital implementation environment and Custom Designer are seamlessly integrated, creating a unified solution that provides lossless roundtrip custom editing of digital designs at any stage of the IC Compiler implementation flow. Design teams can implement custom high-precision edits of IC Compiler designs by easily moving between these digital and custom implementation flows, while maintaining complete design data integrity (see Figure 3). This unified solution accelerates the design development cycle by enabling quick and reliable custom edits to IC Compiler designs at any stage of development, including the time-critical tapeout phase. Typical applications include:

- Precise preplacement of analog macros and adjacent standard cell placement regions
- Creation of complex supply and ground structures
- Pre-routes of critical nets and special nets such as wide, differential, fully-shielded, and matched length or resistance
- Late-stage editing for final DRC, DFM and ECO needs
- Addition of manufacture structures such as probe pads, mask markings, and seal rings

Figure 3: IC Compiler Custom Co-Design
High-performance SPICE and FastSPICE Simulators

HSPICE®, the industry’s “gold standard” for accurate circuit simulation, is tightly integrated with the Custom Designer Simulation and Analysis Environment (SAE). Custom Designer SAE includes a built-in netlister and simulation job control for HSPICE, as well as an HSPICE output file post-processor. All HSPICE simulation results can be displayed in both the tabular SAE simulation summary and in the Custom WaveView waveform viewer. Simulation results can be fully cross-probed between the waveforms, schematic and analysis results display.

For FastSPICE simulation, CustomSim™ delivers superior transistor-level verification performance and capacity for all classes of design, including custom digital, memory and analog/mixed-signal circuits. CustomSim also provides a comprehensive suite of analysis features that includes:

- Static and dynamic circuit checks (see Figure 4)
- CustomSim reliability analysis and visualization for EM and IR-drop analysis
- MOS aging analysis

Both EM and IR-drop analysis are tightly integrated with Custom Designer, allowing reliability analysis visualization in Custom Designer layout view. CustomSim's EM and IR-drop analysis results are displayed in a browsable, spreadsheet-like display with polygons color-highlighted in Custom Designer LE according to the user-specified binning and color map. Violations may be browsed in Custom Designer LE via both a text browser and by color highlighting of the layout (see Figure 5). These browse and display features make it easy to locate and fix IR and electromigration issues. Violations can also be filtered by extracted layer.

High-performance Mixed-Signal Simulation

CustomSim is tightly integrated with Synopsys' VCS® RTL verification solution through direct-kernel integration. This mixed-signal solution improves throughput by breaking through the analog performance bottleneck with the highest-performance circuit simulation technology. A flexible usage model allows for any mixture of abstraction levels and design hierarchy, with full language support for Verilog, VHDL, Verilog-AMS and SPICE. Post-layout simulation is supported through DSPF, SPF, and SDF formats. Digital verification techniques have been extended to transistor-level blocks through a unique integration between CustomSim and VCS. This integration enables verification engineers to create analog assertions, self-checkers and generators within SystemVerilog testbenches. CustomSim and CustomSim-VCS are also integrated with CustomExplorer™ Ultra, a unified AMS verification environment for advanced regression verification and analysis.

Figure 4: CustomExplorer Ultra Integrated with CustomSim Circuit Check
Advanced AMS Regression and Analysis Environment

CustomExplorer Ultra provides an advanced regression and analysis environment for both FastSPICE and mixed-signal verification (see Figure 4). While Custom Designer SAE provides a highly-interactive solution for circuit design and block authoring, CustomExplorer Ultra’s high-productivity verification environment addresses mixed-signal regression testing at the block and block-assembly levels. CustomExplorer Ultra combines simulation setup and job control (including LSF and grid support), multiple testbenches and corners configurations, results analysis, waveform comparison, and debug to significantly reduce the complexity of mixed-signal verification tasks. CustomExplorer Ultra is seamlessly integrated with both CustomSim and CustomSim-VCS mixed-signal simulators for the highest verification speed. Multiple testbench and corner configurations can easily be set up and simulation jobs are automatically queued and submitted to the server farm. Simulation job distribution and monitoring gives real-time status of multiple jobs running on multiple machines, providing quick feedback if problems are detected during simulation.

Integrated Physical (Signoff) Verification and RC Extraction

For signoff DRC/LVS, IC Validator delivers excellent scalability for efficient utilization of available hardware, superior ease-of-use for the physical designer, and high-programmability for easier runset development. IC Validator is seamlessly integrated with Custom Designer to significantly reduce total physical verification time. Designers simply run IC Validator as part of the Custom Designer environment to quickly perform physical verification directly from the OpenAccess database without having to stream out. All detected LVS and DRC errors can be viewed and cross-probed directly in Custom Designer LE, allowing errors to be quickly corrected. IC Validator is fully qualified for DRC/LVS signoff at all leading foundries.

StarRC™ Custom is the gold standard for post-layout parasitic extraction. StarRC Custom combines ScanBand™ pattern-matching technology and Rapid3D fast field solver technology into a single solution that delivers high-performance RC extraction, with tuned accuracy to meet the stringent demands of custom designs. In addition, StarRC Custom’s comprehensive offering includes seamless integration with Custom Designer and optimized links with the CustomSim simulator, enabling increased designer productivity resulting in overall faster time-to-tapeout.

StarRC directly reads the LVS results from IC Validator, avoiding time-consuming stream-out, and performs the parasitic extraction. StarRC then directly writes a layout-extracted view to OpenAccess without having to use an intermediary file such as DSPF. The extracted view can then be directly accessed by Custom Designer and nets or points queried for parasitic information. The extracted layout view can also be cross-probed with the schematic for detailed circuit tuning and debugging.

Figure 5: CustomSim Reliability Analysis and Custom Designer Visualization of IR-drops
Mixed-Signal IP Portfolio

As part of Synopsys' unified solution for custom design, Synopsys offers a leading portfolio of high-quality, silicon-proven IP solutions for SoC designs. Synopsys' DesignWare® IP portfolio includes a complete collection of interface IP solutions consisting of controllers, PHY and verification IP, analog IP, embedded memories, logic libraries, processor cores and SoC infrastructure IP. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. All Synopsys analog IP is developed using the Synopsys custom solution tool suite.

Summary

Synopsys' custom solution provides a highly integrated, single-vendor tool suite for custom and cell-based design and verification. This advanced set of interoperable tools and capabilities dramatically shortens time-to-tapeout, improves design quality, and enables mixed-signal SoC design at the most advanced process nodes.