White Paper

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In-Design Rail Analysis™ Accelerates Power Network Closure

September 2009

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Introduction

In today's complex system-on-chip (SoC) designs, static and dynamic voltage-drop and electromigration (EM) effects are increasing. At 90 nanometer (nm) and below, these effects are having a profound impact on timing, contributing 10 to 15 percent delay sensitivity and overall design viability. Due to the performance sensitivity to power and ground (P/G) noises, rail analysis solutions that have been used in high performance networking, wireless/mobile or low-power consumer applications become critical for all design applications at advanced process nodes. These applications are facing challenges of increasing power network failures that are resulted from the increased power and current densities, technology and voltage scaling, larger die sizes, higher variance, and so on.

With the increasing demands on rail analysis solutions and the complexity of the designs, the existing rail analysis solutions of checking designs upfront or at the tape-out stage are no longer sufficient. IC designers need a rail analysis solution that can easily analyze and optimize power and ground (P/G) network at any stage in the implementation flow. The solution needs to be easy to use, requires minimal setup, and provides intuitive graphical user interface for debugging, fixing, and refining. Most of all, the solution has to fit with their existing implementation flow and yet offers comprehensive P/G grid analysis.

Synopsys In-Design Rail Analysis solution is implemented to meet this demand by offering a tight integration between PrimeRail and IC Compiler. With this In-Design Rail Analysis solution, IC designers can run rail analysis at any design phase, from design planning, placement, routing to final sign-off. Rail analysis setup and analysis result viewing can be easily done in the IC Compiler environment. Consequently, design closure can be achieved sooner without making power network changes at the end of design cycle when these changes become more intrusive.

Existing Rail Analysis Approach

Shown in Figure 1, the present power network design flow consists of separate implementation and verification steps, often performed by different engineers using different tools in various environments. In leading-edge system-on-chip (SoC) designs, this often results in excessive iterations between physical implementation and signoff, consequently jeopardizing project schedules. In addition, at leading-edge nodes like 65nm and below, this "implement-then-verify" approach is slow and may complicate convergence when rail fixes can alter design objectives, such as area, timing and power.

Three key problems are associated with the existing rail analysis approaches:

- Place and route designers not focusing on rail analysis
- Different database and views
- Late-stage surprise

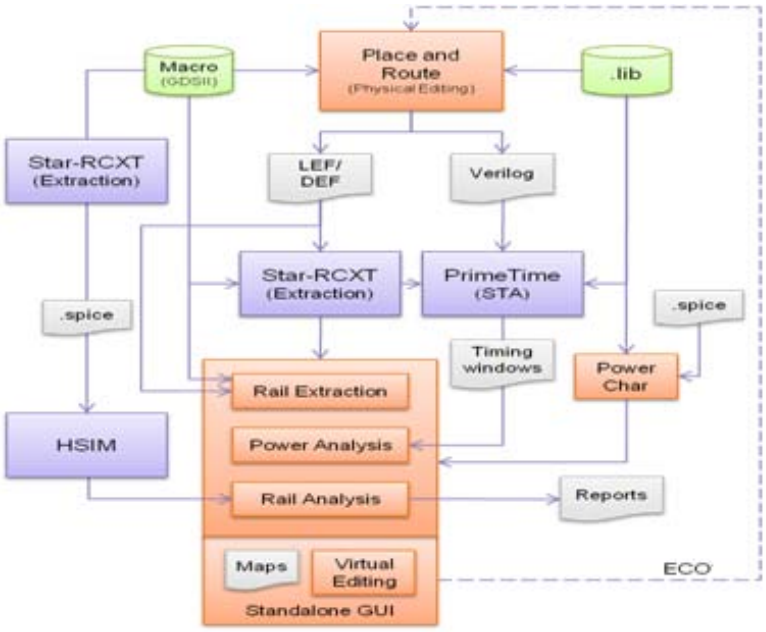

Figure 1: Bolted-On Rail Analysis Flow

Place and Route Designers Not Focusing on Rail Analysis

Under fast time-to-market pressure, place and route designers rely on over-design of the power network to achieve design closure as quickly as possible. The designers tend to use lower supply voltages to reduce noise margins, which does not help reduce IR drop problems but may cause more chip failures than before.

In the existing rail analysis method, physical designers do most of the implementation tasks in a place and route tool, including floorplanning, power rails laid down, placement, clock designing, and detailed routing. When designers want to verify the power network for IR drops and electromigration effects, they have to leave the place and route environment and run rail analysis in a rail analysis tool. This is time-consuming and effort taking because each verification and fixing cycle requires a separate trip between place and route and rail analysis tools.

Different Database and Views

Because most "place and route" and "rail analysis" tools use different database, there is a translation step required. Thus, when the bolted-on rail analysis identifies a power network issue, designers first need to fix it in the rail analysis database. After the power network design is verified to be robust in the rail analysis tool, the same changes need to be done in the place and route tool. Moreover, working among multiple databases requires data translations. The productivity is greatly reduced because designers need to resolve file format and version compatibility issues among different tools.

Late-Stage Surprise

In the existing rail analysis method, physical designers usually run rail analysis till it is closer to tape-out. When a power network issue is identified late in the design flow, fixes required may be intrusive and designers may need to rework on the design to avoid area, timing, and power violations. This can significantly delay the tape-out schedule and increase the overall turnaround time.

Synopsys IC Compiler In-Design Rail Analysis with PrimeRail Technology

By eliminating complicated data exchanges and with no new tools to learn, IC Compiler users can now ensure the integrity of their power network early and as frequently as desired during the physical implementation process, avoiding late-stage surprises close to tape-out. Shown in Figure 2, In-Design Rail Analysis works in tandem with IC Compiler's Power Network Synthesis (PNS) capability to enable designers to efficiently implement, debug and refine power networks which significantly reduces the possibility of over-designing. In addition, the In-Design Physical Verification flow in IC Compiler also helps ensure that power networks are design-rule clean as refinements and fixes are implemented. IC Compiler's ecosystem of PNS, In-Design Rail Analysis and In-Design Physical Verification offers the fastest and most comprehensive solution for power network designs.

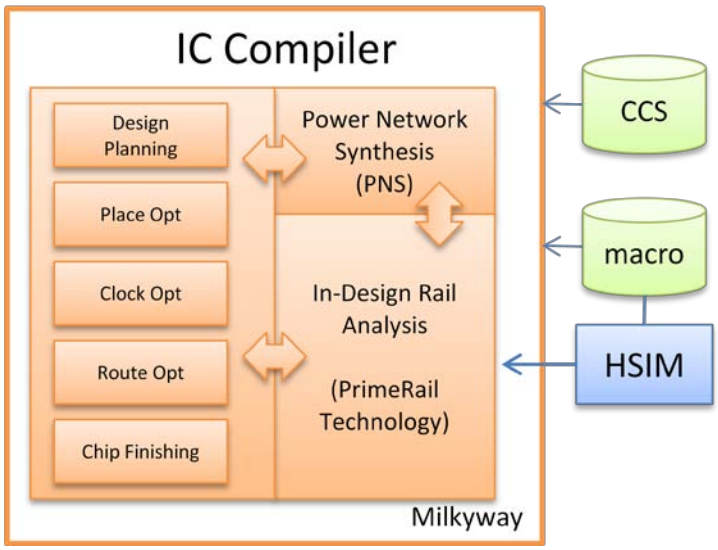

Figure 2: IC Compiler In-Design Rail Analysis with PrimeRail Technology

In-Design Rail Analysis offers the following benefits:

- Early Detection and Fixing Guidance:

With in-Design Rail Analysis, physical designers can run rail analysis at any design stages when design planning is done, without leaving the IC Compiler environment. In-Design Rail Analysis reports possible problems found and provides fixing recommendations for designers, who can then fix the problems in the editable layout right away, thereby saving a significant amount of time.

- No Data Exchange Between Tools:

The In-Design Rail Analysis flow within IC Compiler eliminates the need for importing and exporting data between place and route and rail tools. Error cells and rail views are created for debugging and viewing analysis results in IC Compiler. IC Compiler Error Browser uses error views to communicate fixing guidance.

- Integrated Flow:

Tight integration between IC Compiler and PrimeRail provides an easy way for customers to reach power and ground grid closure for both static and dynamic analysis.

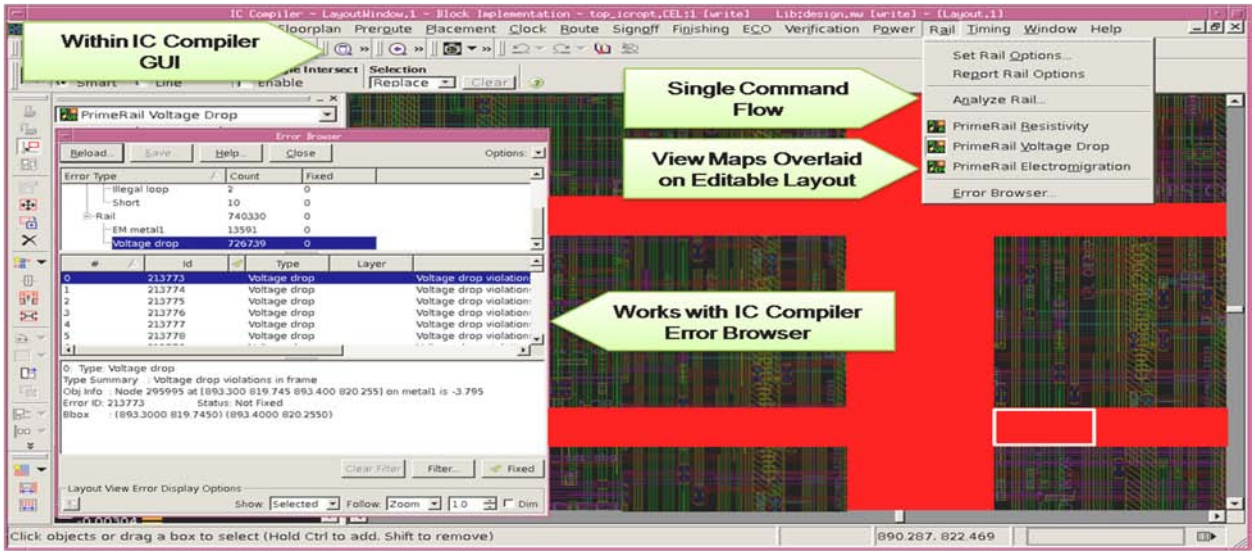

Figure 3: The Integrated Rail and Place and Route Environment

- Static In-Design Rail Analysis

Static In-Design Rail Analysis provides multiple analysis features: rail integrity checking, resistivity analysis, static IR drop analysis, and static electromigration (EM) analysis. For example, users can do rail checking to get connectivity and resistivity information. If there is high resistivity in the map, it can either be a connection issue or a missing pad. A connection issue can be caused by unconnected cell instances,

floating geometries (disconnected wires and vias), and possible missing vias. Missing pads can be resulted from the fact that the area is too far away from the supply voltage and a pad needs to be added.

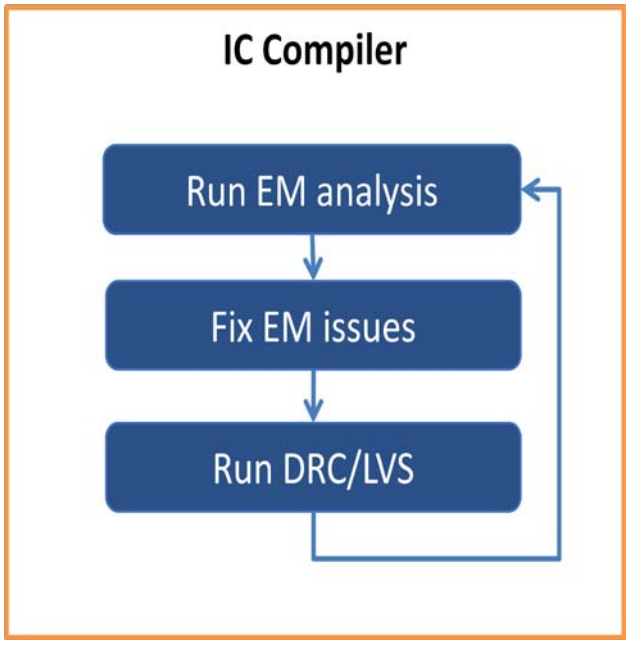

Figure 4 In-Design EM Analysis Flow

Figure 4 shows the static EM analysis flow in IC Compiler. Electromigration (EM) is the motion of atoms in response to the electron "wind", i.e., momentum transfer with the electrons pushing the atoms. This can eventually cause opens or shorts and long term deterioration of the wire's electrical characteristics. EM analysis and fixing helps prevent reliability problems caused by any possible metal migration and thermal expansion failures. In-Design Rail Analysis identifies EM violations for a power and ground net or a supply net. One way PrimeRail uses to report EM issues is through a visual display of a colored range of EM values overlaid on the physical supply nets; this is commonly referred to as an EM map. EM maps can be directly viewed in IC Compiler, as illustrated in Figure 3. Another way is with an error cell which contains EM violations and a text report for fixing suggestions. EM violations are available in IC Compiler Error Browser, which also includes In-Design Rail Guidance. In-Design Rail Guidance can be used to address any possible violations on the editable layout in IC Compiler. After any EM-based design modifications are completed inside of IC Compiler, users should iterate this EM analysis process with In-Design Rail Analysis to ensure that all the EM violations are handled. Users can also use In-Design Physical Verification to confirm the fixes are DRC clean.

- Dynamic In-Design Rail Analysis

The static In-Design Rail Analysis is available in IC Compiler version C-2009.06 and after. The dynamic In-Design Rail Analysis will be available sometime later this year, although dynamic rail analysis is a long supported feature in the stand-alone version of PrimeRail. One of the most widely used techniques to reduce peak dynamic IR voltage drop on power supplies is to add decoupling capacitance (decap) cells in the affected area; however, decap insertion introduces leakage. In-Design Rail Analysis can minimize peak dynamic IR drop at a minimum decap insertion cost. This cost is based on the available area for decap insertion and is measured so as to minimize the needed capacitance, area and leakage. Shown in Figure 5, it first looks at the preplaced filler cells in the design and then virtually replaces all of them with decap cells. The filler area is used as the candidate area for decap cell swapping. It considers user-target peak reduction and leakage to reduce the number of inserted decap cells. When analysis is complete, In-Design Rail Analysis provides suggestions for decap insertion, and an ECO file is generated. With the tight integration between IC Compiler and PrimeRail, the ECO file can be used as an input to IC Compiler which automatically inserts these new cells and places them while swapping out the existing filler cells. The placed decap cells are guaranteed to be DRC clean.

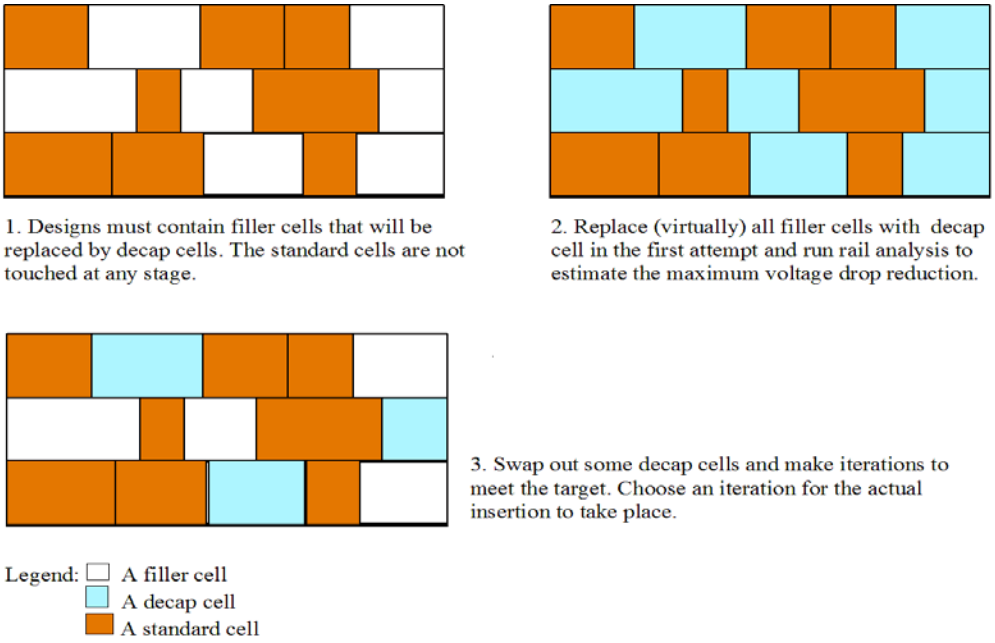

Figure 5: Decap Insertion Flow

Summary

Finding power grid issues in the late stages during the physical implementation process can lead to painful rip-up and repair iterations. Architected for place and route engineers, IC Compiler In-Design Rail Analysis with PrimeRail technology enables you to analyze, identify, and fix potential problems without leaving the IC Compiler environment. In-Design Rail Analysis directly accesses the Milkyway database while creating Error cells and rail views for debugging and analysis result viewing. Utilizing PNS features in IC Compiler, In-Design Rail Analysis accelerates the path to the final power network closure with In-Design Rail Guidance.

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