White Paper

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Test Automation of 3D Integrated Systems

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Introduction

Advances in packaging technologies have led to the development of three-dimensional (3D) integrated systems that offer the potential to deliver significant improvements in performance, power, functional density, and form factor over systems that rely on standard packaging integration techniques. Although the design and test requirements for these highly integrated systems are still evolving, it is evident that advanced test automation will be essential in ramping 3D systems to volume production. This whitepaper discusses some of the key test challenges related to 3D integrated systems, and how Synopsys' synthesis-based test solution can be used to rapidly address these challenges.

2.5D and 3D Integration

Two basic types of 3D packaging configurations have emerged. "2.5D" integration mounts multiple two-dimensional (2D) dies atop a common electrical interface, called a silicon interposer, and connects them together with wires that run through the interposer (Figure 1). The system I/Os are connected to the underlying package substrate using vertical Through Silicon Vias (TSVs) that extend partway through the interposer. A system of three-dimensional stacked ICs (3D-SICs) (Figure 2) achieves an even tighter form factor than 2.5D integration. In this configuration, TSVs are etched deep into the substrate and wafers comprised of 2D ICs are thinned down to less than 50 microns. Multiple dies are then stacked vertically and connected by TSVs.

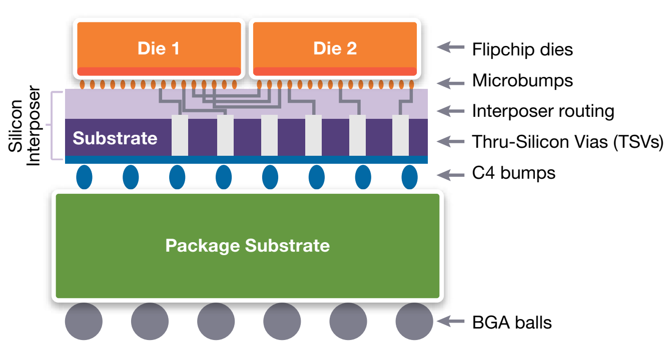

Figure 1: 2.5D integration with two dies connected by wires running through a silicon interposer

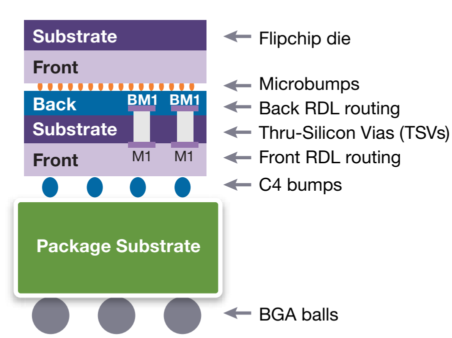

Figure 2: 3D-SICs with two stacked dies connected by TSVs

Testing stacked configurations requires a superset of the automation needed for testing 2.5D packages, and is the focus of the discussion in the sections that follow.

Testing 3D Stacked ICs

Figure 3 illustrates two of many possible 3D-SIC test scenarios for a hypothetical three-die stack. One approach is to perform a stack test after all the dies have been bonded together, as illustrated in the first scenario. The stack test begins with a TSV interconnect test between the bottom (first) die and second die, and between the second die and third die, followed by testing of each die in sequence starting from the bottom die. Stack testing can also involve testing the entire stack simultaneously as an integrated system.

Because it is not viable to "un-bond" a die subsequently found to be defective, performing a separate Known Good Die (KGD) test for an individual IC prior to bonding may be more cost-effective than relying solely on stack tests to identify a defective die that has already rendered the entire system defective. In the second scenario of Figure 3, a stack test is performed each time a KGD is bonded to the top of the IC stack to screen for damage to the top two dies and their interconnect that might have occurred during the bonding process.

Scenario 1	Scenario 2
1. Test die 1	1. Perform KGD test (die 1)
2. Bond die 2 to die 1	2. Perform KGD test (die 2)
3. Bond die 3 to die 2	3. Perform KGD test (die 3)
4. Test stack of dies 1, 2, 3:	4. Bond die 2 to die 1
1. Test die 1-2 TSV interconnect	5. Test stack of dies 1, 2:
2. Test die 2-3 TSV interconnect	1. Test die 1-2 TSV interconnect
3. Test die 1	2. Test die 1
4. Test die 2	3. Test die 2
5. Test die 3	6. Bond die 3 to die 2
	7. Test stack of dies 1, 2, 3:
	1. Test die 2-3 TSV interconnect
	2. Test die 2
	3. Test die 3

Figure 3: Example 3D-SIC test scenarios for a three-die stack. In the first scenario, a stack test is performed only after bonding of all three dies. In the second scenario, a stack test is applied each time a Known Good Die is bonded to the top of the stack.

Known Good Die Testing

Although incorporating KGD testing into a 3D-SIC test flow has the potential to reduce total manufacturing and test costs, it comes with a unique set of challenges. With the exception of the bottom die, no probe pads exist for KGD testing because all the I/Os are accessible only through TSVs topped by fine-pitch micro-bumps, arrayed on both sides of the die. Industry efforts are underway to build probe systems that address these constraints, but until the new systems are production-ready designers must consider other methods that leverage their existing automatic test equipment (ATE) infrastructure. One viable approach is insertion of "sacrificial" probe pads used only for KGD testing. Although there is a silicon area overhead penalty associated with the dedicated probe pads, it is possible to minimize the number of pads by using the pin-limited test feature in DFTMAX compression. Pin-limited testing reduces test application time and test data volume up to 170X, utilizing as few as one pair of test data pins.

In addition, since fault effects in 3D-SICs appear to be identical to those encountered in 2D designs, conventional fault models can still be used when generating KGD test patterns. However, because 3D integrated systems offer smaller form factors and higher performance than conventional designs, more advanced tests available in TetraMAX ATPG—for example, slack-based transition delay tests that target small delay defects and bridging tests that target bridging faults—may be required for high-quality KGD testing.

Even so, scan testing alone is not sufficient. Many thousands of TSVs are used for connecting adjacent dies, and their faults are not observable during KGD testing without probe technology that can accommodate the fine-pitch requirements of 3D-SICs. Designers can overcome this obstacle by using bidirectional I/O wrapper cells for all the TSV I/Os. TetraMAX can model the I/Os as bidirectional pins and then generate TSV "loopback" tests that allow data to be applied to and captured from the TSV I/Os to verify their functionality.

Defect-driven embedded memory self-test and repair is another key component of KGD testing. Designers of 3D integrated systems can implement Synopsys' DesignWare Self-Test and Repair (STAR) Memory System to achieve the highest defect coverage of Synopsys and third-party memories.

Power Considerations

Greater system complexity of 3D-SICs demands tighter control of dynamic power consumption, which differs before and after a die is bonded to a stack (since TSVs distribute power up the stack in the latter case). Advanced power management techniques such as power-aware ATPG and power domain-based test are needed to limit power consumption and thereby minimize false failures during 3D-SIC testing. With power-aware ATPG, DFTMAX and TetraMAX work in tandem to produce patterns that limit both shift mode and capture mode power to functional levels based on a designer-specified flop switching budget. With power domain-based test, TetraMAX generates patterns in compliance with a design's functional power states to reduce both dynamic and leakage power and minimize IR-drop issues. It also further increases defect coverage by generating pattern sequences that test the power management circuits. Synopsys' advanced power management capabilities have been successfully deployed with 2D designs to improve defect coverage and limit false failures on the ATE, and will be essential for 3D-SIC testing.

Stack Testing

Once the KGD patterns are generated by TetraMAX, mapping them to stack-level ports is a straightforward process. For TSV interconnect tests, TetraMAX uses dynamic bridging fault models to generate at-speed patterns that can target time-sensitive shorts between TSV I/Os. But the main challenge of stack testing is designing and implementing a 3D DFT architecture that provides adequate test access to non-bottom dies for performing individual die tests, inter-die (i.e., TSV interconnect) tests, and possibly simultaneous multi-die tests. Synopsys is actively participating in the development of emerging 3D test access standards such as IEEE P1838. Although these standards have not yet coalesced, it is possible for early adopters to use Synopsys' synthesis-based test solution to efficiently implement 3D DFT architectures that are based on established standards.

For example, DFTMAX can synthesize, connect, and verify the JTAG Test Access Port (TAP) and boundary scan register (BSR) logic for 3D-SIC systems that utilize IEEE Std 1149.1 as a test access mechanism for performing either KGD or stack testing. DFTMAX also leverages IEEE Std 1500 for core wrapping and for "die wrapping"—when the test control interface for non-bottom dies makes use of IEEE Std 1500-based wrappers. Similarly, the DesignWare STAR Memory System, residing on the bottom die and receiving its instructions via the JTAG TAP, can utilize IEEE Std 1500 interfaces to provide the necessary test access and isolation for memories embedded in all other dies in the stack. Once the test interfaces are implemented on each die, they are daisy-chained up and down the stack to enable stack testing of both logic-on-logic and memory-on-logic configurations, as shown in Figure 4.

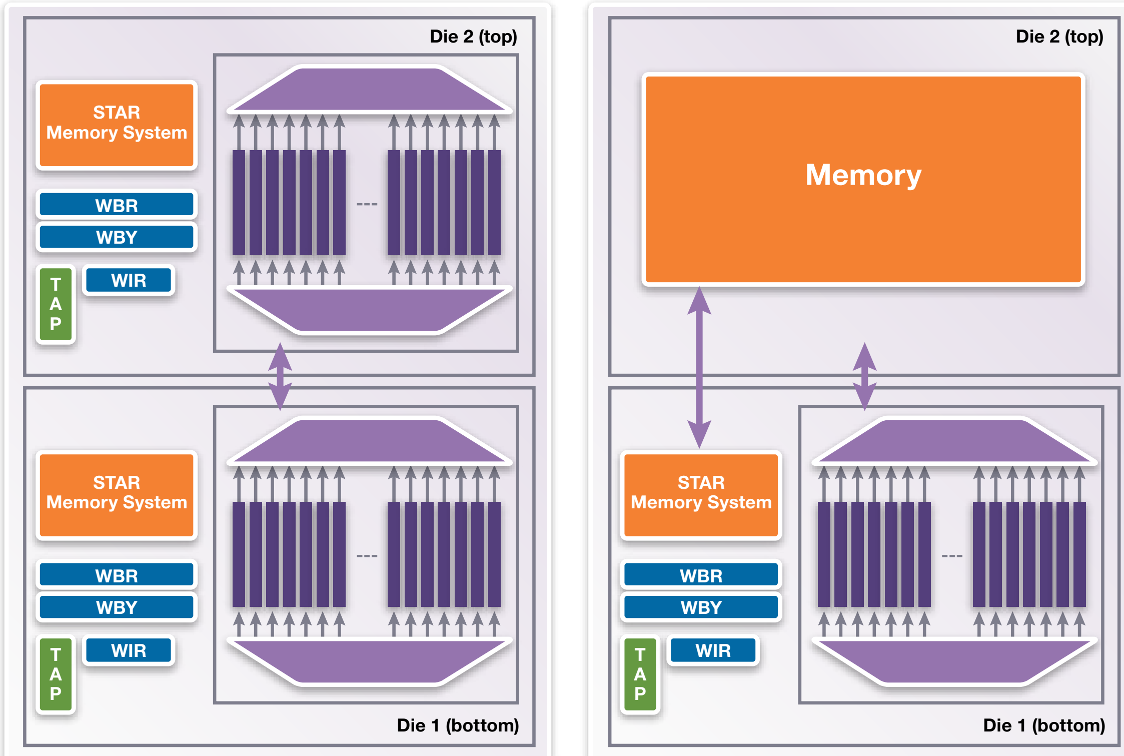

Figure 4: Synopsys supports 3D-SIC testing for both logic-on-logic and memory-on-logic systems based on established test access standards.

Another capability that provides access to embedded test and debug resources in 3D-SICs via the JTAG TAP is the DesignWare SERDES IP (UPx). Synopsys' self-test of high-speed interfaces seems to be compatible with the emerging IEEE Std P1687, the proposed instrumentation standard, and is an example of the type of instrument access mechanisms that are critical for successful 3D-SIC product certification and deployment. In addition to the standards already mentioned, Synopsys' test solution employs STIL (IEEE Std 1450.x) and CTL (IEEE Std 1450.6) as mainstream interfaces to other systems in the electronics design and manufacturing industry, and as means to enable testing of both 2.5D and 3D packaging configurations.

Summary

High-quality, economical testing of 3D integrated systems requires a comprehensive set of leading-edge test automation technologies, including pin-limited scan compression, power-aware ATPG, power domain-based test, slack-based at-speed test, dynamic bridging test, defect-driven embedded memory self-test and repair, and self-test of high-speed interfaces. These technologies are all available today and fully integrated in Synopsys' synthesis-based test solution, comprised of DFTMAX, TetraMAX, and DesignWare IP. Although 3D test access standards have not yet converged, early adopters can already use the Synopsys test solution—proven effective at testing thousands of complex 2D systems—to maximize their design productivity when implementing test for 3D systems.

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