

Synopsys and STMicroelectronics Noida

ST Noida Quickly Achieves Advanced Video Compression with Synphony C Compiler



Even with no RTL experience, we were able to complete this complex digital video hardware IP design in 9 months with two engineers.”

Ravin Sachdeva

Technical Leader, STMicroelectronics



Business

STMicroelectronics is a global semiconductor company producing a diverse range of devices, ranging from single transistors to microprocessors and complex SoCs. The ST Noida site focuses on the design of home video products.

Challenges

- ▶ Meet target QoR expectations for RTL output despite no prior experience with RTL
- ▶ Use unique SCC hierarchical optimizations to achieve efficient HW
- ▶ Explore architecture early and quickly

System-Level Design Solution

- ▶ Synphony C Compiler high-level synthesis tool

Benefits

- ▶ Automated flow from complex C/C++ & hardware to highly optimized RTL
- ▶ High QoR exceeding performance and area goals
- ▶ Low effort required with easy learning curve

Overview

A team at ST Noida working on multimedia embedded software/hardware needed to create a complex digital video hardware IP block. The team of two software algorithm engineers was very strong in writing C algorithms; however they had limited exposure to hardware design and no prior experience with RTL.

The project was for one of the Entropy Decoding schemes in H.264, Context Adaptive Binary Arithmetic Coding (CABAC) with a target for use in 45nm CMOS to achieve real-time video for HDTV systems. The team needed a maximum gate count of under 200 K gates and a clock speed of 200 MHz. They also needed one bin per cycle processing from the Binary Arithmetic Decoder block meaning each bin must complete in one clock cycle to guarantee real-time performance.

CABAC decoding consists of three main stages: 1) contest modeling, 2) binary arithmetic decoding, and 3) debinarization. Because there is a high internal data dependency between the three stages, the CABAC is difficult to pipeline/parallelize and can prevent the design from reaching a high throughput. The architecture contains 15 main blocks.

Leading High-Level Synthesis Solution

The ST Noida team chose Symphony C Compiler for four main reasons. First, because the team has expertise in C, they needed a high-level synthesis (HLS) tool that used C as the input language. Not only does Symphony input C/C++, but the tool's C support is extensive and covers almost all of the C syntax and semantics they used.

Second, Symphony C Compiler allowed the team to quickly specify and explore different architectures for hardware implementation. They could directly modify the algorithm to accommodate specification changes – the cost of which is much lower than modifying RTL. Plus, they were able to incorporate future revisions and spec changes efficiently.

Third, the team's customers – other internal groups – previously had to convert the optimized algorithms into C and then into RTL themselves. Using Symphony saved time and effort for this handoff. The tool was easy to integrate into their flow.

And fourth, Symphony C Compiler enabled a high level of productivity not found with any other HLS tool. Symphony provided various levels of verification steps including Lint Simulation, SystemC simulations, and RTL simulations allowing the team to recognize bugs early in its integrated design and verification flow.

The tool also features Tightly-Coupled Accelerator Blocks (TCABs), which allows unlimited hierarchy so teams can create blocks and use them throughout the design. Using TCABs, the SCC high-level synthesis engine can achieve very efficient area optimizations using resource-sharing and scheduling of complex hierarchical C/C++ code. The ST Noida team used this feature to optimize resource sharing with multipliers. They used 2-3 levels of TCAB hierarchy for the chip's 15 blocks, comprised in 17 Symphony C Compiler TCABs. The team was able to meet their performance goal only because they were able to optimize the Arithmetic Decoder (their design core) using the TCAB feature and share this hardware across many blocks.

With unlimited code input, Symphony C Compiler also completed all the timing and clock generation while meeting performance goals with good QoR.

The results exceeded performance and area goals with 185K gates, 222 MHz in 45nm technology.

With this project successfully completed, the ST Noida team has now started a new project and will continue to use Symphony C Compiler.

“Symphony C Compiler let us easily explore different implementations for the same design and quickly find the best tradeoffs in power, performance and area.”

Ravin Sachdeva
Technical Leader, STMicroelectronics



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