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Deploying a Convergent 10-nm Design Flow with IC Compiler II

Along With Other IC Design Leaders Like Intel, Mellanox and Samsung, Broadcom Participated in the 2016 IC Compiler II Technology Symposium in Santa Clara, CA. This Is a Brief Recap of the Broadcom Presentation.

10-nm: The Promise, the Challenges and the Solution

In the semiconductor market, mobile applications with large revenue potential and high volume are the key drivers for the migration to advanced technology nodes. The need for higher performance combined with the requirement to maintain power consumption at the same level as the previous technology node is key. At 10 nanometers, smaller feature size enables higher density, more functionality, and a smaller footprint. These benefits are not free, as they pose serious technology challenges during physical implementation and signoff; they are multi-dimensional and include increased parasitics and complex interconnects with more sensitivity to variations in wafer process and temperature. The Broadcom SoC group developed a 10-nm based flow using IC Compiler II that successfully addresses these challenges.

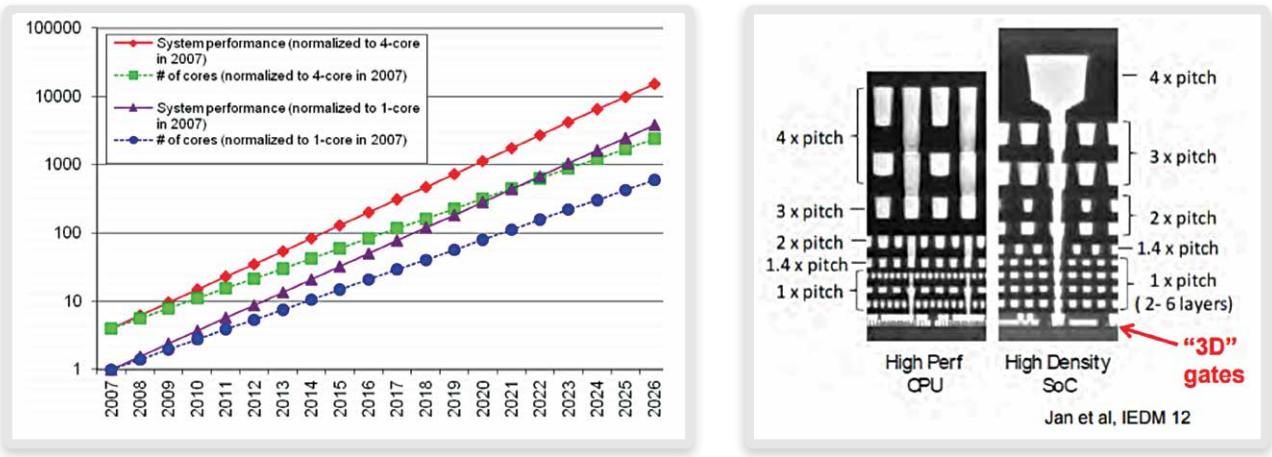

Figure 1. Increased design complexity driven by faster performance, heterogeneous layer stacks and 10-nm DPT requirements

Broadcom's IC Compiler II-based 10-nm Flow

Broadcom developed a holistic flow using multiple designs at 10-nm, with clock frequencies up to 2GHz+, 2M+ cells, and 150+ macros, including complex floorplans dominated by both macros and logic. The four areas of focus were: design complexity, managing routability, timing optimization, and design convergence.

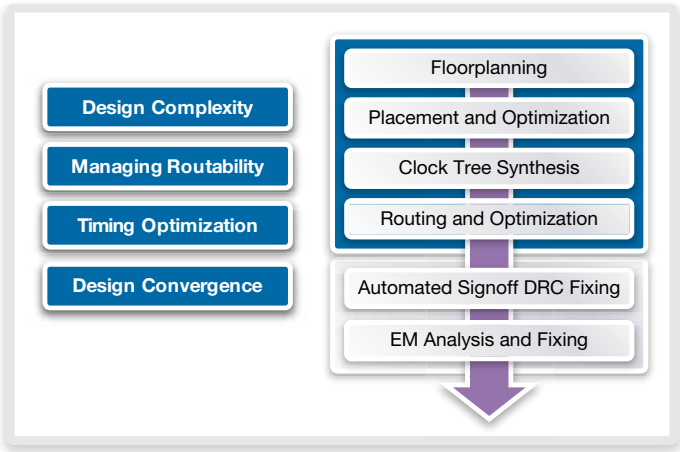

Figure 2. 10-nm design flow. Four focus areas and physical implementation and signoff

Technology-based Convergent Flow

Design Complexity: Modern SoCs have large on-chip memory. Using tiling techniques, designers broke apart the large memories into smaller pieces and then used tiling to create a more optimal floorplan. This floorplan had paths from I/O pins to memories that traversed through multiple levels of pipeline registers. IC Compiler II's connectivity-based register tracing capability improved the placement and the floorplan. Memory fragmentation and register tracing capabilities were instrumental in meeting memory-to-register and register-to-memory timing and ensuring that the design was routable.

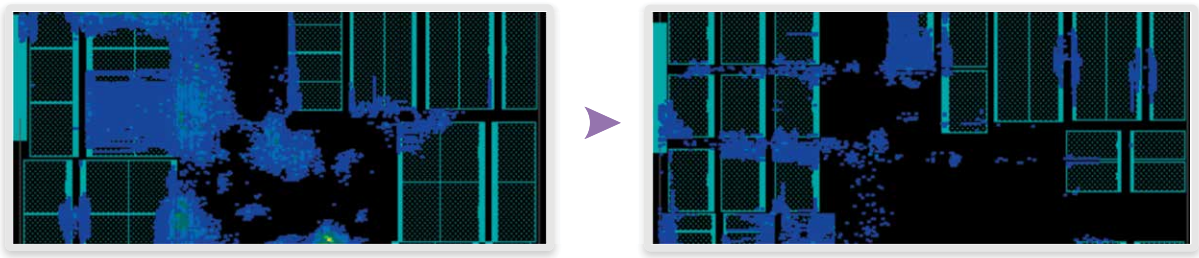

Figure 3. Reduced congestion and improved memory-to-logic and logic-to-memory WNS

Managing Routability: The congestion in the standard cell core area was challenging in this design. The smaller device sizes lead to a routing resource crunch, along with the usage of complex cells, multiple levels of design hierarchy, and higher fan-out and fan-in cones. IC Compiler II provided a range of options; keep-outs, cell spreading, bounds, density screening, and incremental placement and optimization techniques. These techniques helped resolve congestion and improved timing.

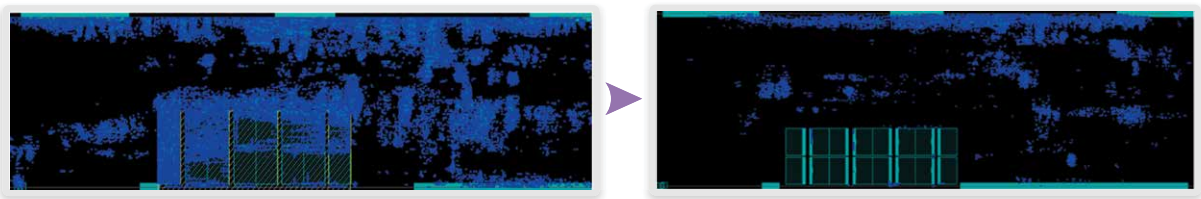

Figure 4. Module bounds reduced congestion and improved register-to-register timing

At 10-nm, the management of congestion and routability is interrelated with buffering and area, and cell choices with tight pin accessibility. DPT layers have 1D routing, coloring, a multitude of rules for line-end, min-area/length, and via-spacing rules. More cells to optimize and a higher cell density requires wider power rails to minimize IR-drop. To address the congestion, Broadcom utilized congestion-driven coarse placement, followed by high-congestion effort during placement, optimization, and clock tree synthesis. IC Compiler II's unique buffer and area reduction techniques coupled with congestion options provided the best results.

Timing Optimization: Concurrent optimization aware of multicorner-multimode (MCMM) and multi-voltage (MV) needs to take into account FinFET characteristics. IC Compiler II's placement and optimization techniques minimized TNS by maximizing slack recovery throughout the logic cone. It handled the heterogeneous layer resistance profiles and intelligently selected devices for optimization based on timing, leakage, dynamic power, and area. Automatic layer-optimization met key design metrics. With increasing utilization and shrinking geometries, designers observed more crosstalk impact, as it degraded timing and affected pre-to-post-route correlation. Broadcom addressed these signal integrity (SI) effects by focusing on the aggressor net or aiding the victim net with an intelligent global route, track assignment, and detailed routing flow. This enabled Broadcom to address the SI violations with minimal use of sparse routing, thus reducing mask cost.

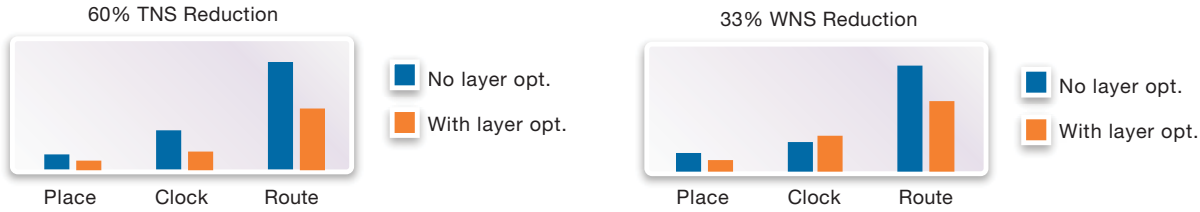

Figure 5. Automatic layer optimization significantly improved the PPA

Design Convergence: With Broadcom's aggressive design schedule it was critical to achieve faster design convergence and closure. Faster design convergence was facilitated by tight place-and-route to signoff correlation and by using In-Design Automated-DRC (ADR) fixing as well as by utilizing IC Compiler II's electro-migration fixing. In 10-nm FinFET technology current density has increased by almost 50% compared to the CMOS planar technology at 20-nm. This has drastically increased the signal EM violations. Using EM analysis and targeting non-default rules (NDRs) based on capacitance thresholds, the EM violations were fixed. 10-nm with DPT, coloring, mask decomposability and the exponential rise in complex rules make manual DRC fixing infeasible. IC Compiler II's In-Design ADR capability with IC Validator fixed more than 95% of the routing and DPT violations and reduced time to closure.

Figure 6. In-Design ADR fixed the routing and DPT violations

Conclusion

Using IC Compiler II, the Broadcom SoC group developed a holistic flow that successfully meets their area, performance and power goals while improving routability. This enables them to achieve faster design closure and successfully deliver designs with aggressive tapeout schedules.

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