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# Designing Next-Generation Mobile Application Processors with IC Compiler II

Along with other IC Design leaders like Intel, Broadcom and Mellanox, Samsung presented at the IC Compiler II Technology Symposium. This is a brief recap of the Samsung presentation.

## Mobile Application Processors: The Leading Edge of Design

Over the last decade, mobile phones have migrated from simple telephones to powerful handheld computers. Enabling this handheld computing revolution, Mobile Application Processors have continuously pushed the boundaries of semiconductor and EDA technology. As the leading supplier of mobile phones, Samsung is at the forefront of Mobile Application Processor development. Samsung uses IC Compiler II from Synopsys to achieve the most stringent Quality-of-Results (QoR) in performance, power and area for their advanced Mobile Application Processor development.

## Challenges of Variability With Advanced-Node FinFET

Designing with FinFET technology at 14nm and below introduces new technology challenges. For example, resistance variability across the layer stack dominates, while capacitance is essentially flat. To address this variability, design tools must be variability-aware and able to compensate for the different layer resistivities.

Addressing this challenge, Samsung used Synopsys' IC Compiler II layer-promotion technology. Layer-promotion for timing and demotion for power made it possible to improve timing significantly and ensure that critical paths gained access to higher, lower-R layers. Using this technology, Samsung saw improved timing, significantly less violations and reduced congestion. The reduction in congestion also made the design easier and faster to route, leading to faster time-to-results.

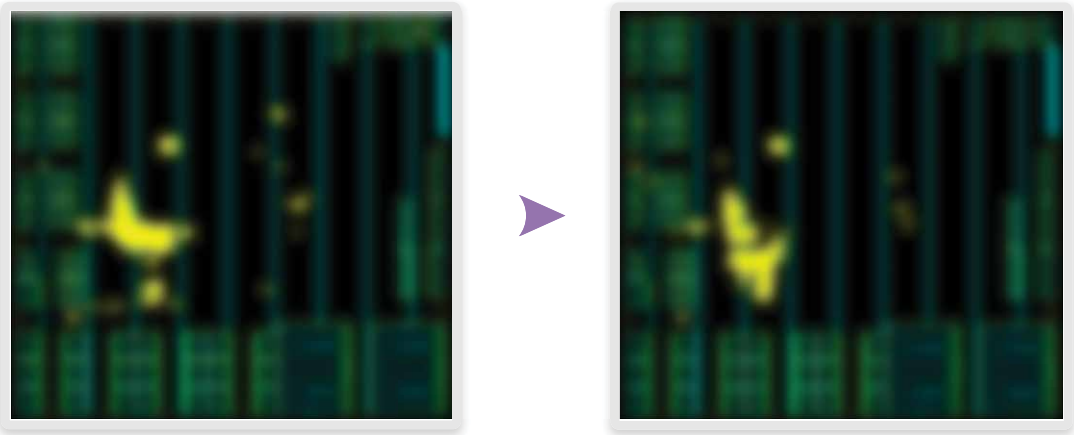

**Figure 1. New layer promotion technology lead to a reduction in congestion**

Another aspect of variability with advanced-node designs is On-Chip Variation (OCV). Without accurate methods to account for OCV, the design will suffer a QoR penalty, especially area QoR. Using IC Compiler II, Samsung evaluated Parametric OCV (POCV) analysis. They saw that IC Compiler II's POCV analysis resulted in excellent correlation with PrimeTime's Path Based Analysis (PBA)-based signoff analysis.

## Optimizing Area While Managing Congestion

In advanced-node designs, Samsung has seen traditional Clock Tree Synthesis (CTS) techniques that use Virtual-Route (VR)-based congestion analysis leading to congestion in the early stages of designs.

The example below is a complex and congested design. VR-based CTS results in congestion hotspots are shown in the left-hand image. This congestion results in thousands of DRCs shown in the right-hand image.

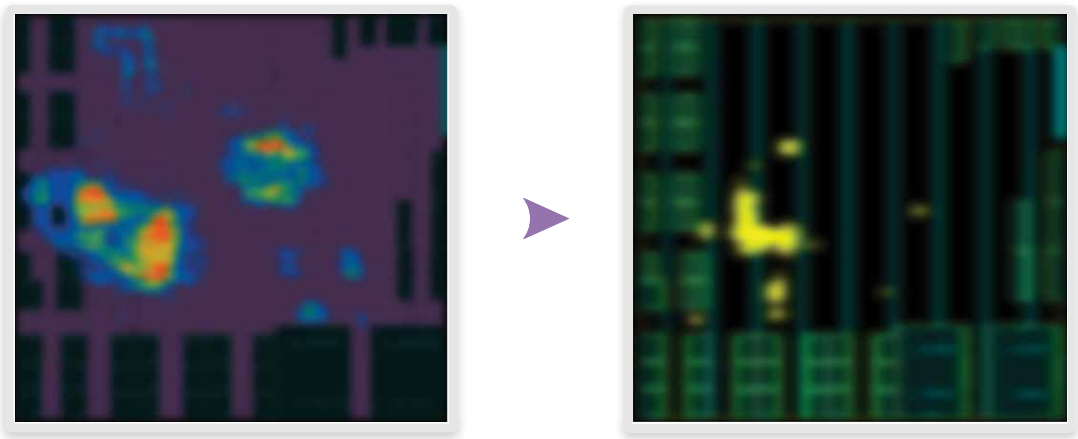

**Figure 2. Congestion and DRCs resulting from Virtual-Route based Clock Tree Synthesis**

Congestion also leads to clock QoR degradation after clock routing which is very difficult to recover in the later stages of place and route. Another challenge is managing placement around highly congested cores, especially as advanced-node pin accessibility is very tight, further impacting routability.

To address clock congestion, Samsung used Global-Route (GR)-based CTS from IC Compiler II. This new capability provided better analysis of congestion during clock construction. On a sample design, routability was improved by 3X while also improving clock QoR and accelerating turnaround time.

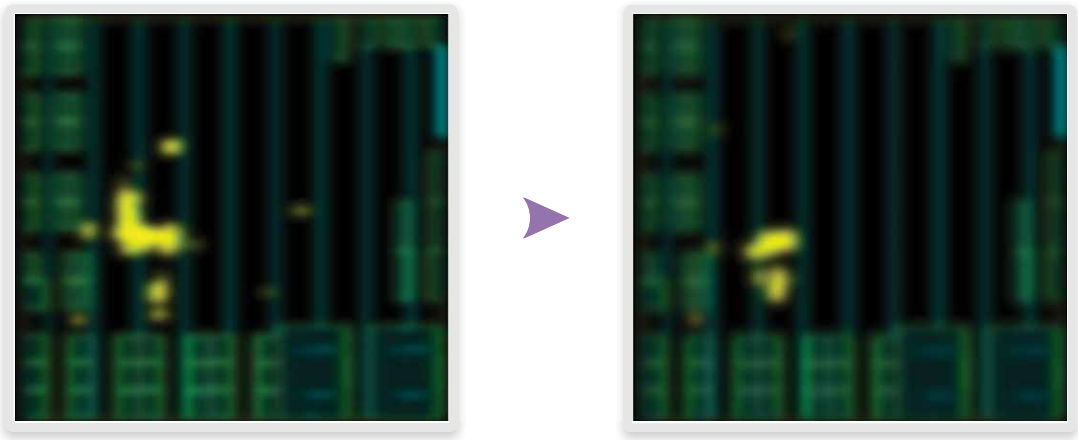

**Figure 3. Reduction in congestion/DRCs using Global Route based CTS**

To further improve routing around highly congested cores, Samsung employed a new IC Compiler II technology called Congestion-Driven Restructuring (CDR). CDR optimizes logic cone connectivity, reducing the amount of crossing wires entering the logic and thus reducing congestion.

CDR produced very strong results for Samsung, as shown in the example below. The image on the left shows congestion that existed without use of CDR. The image on the right shows almost complete removal of congestion hotspots due to IC Compiler II's CDR technology.

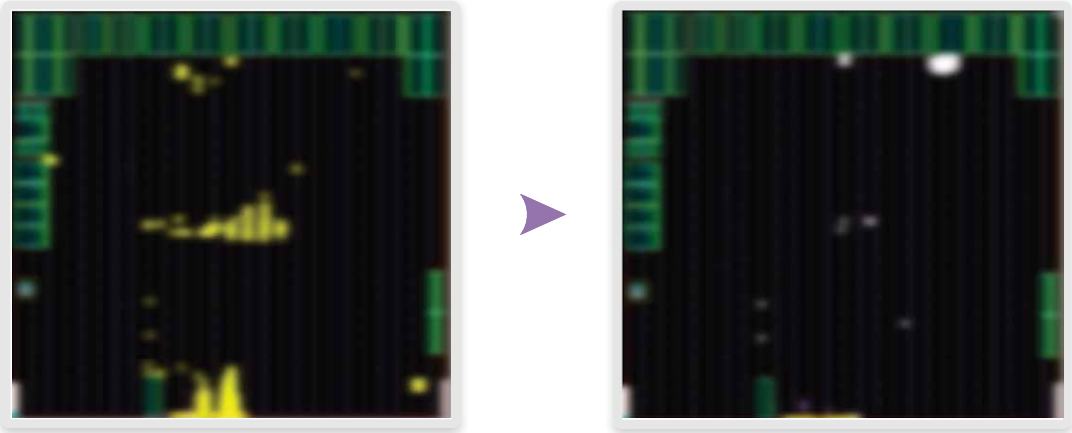

**Figure 4. Reduction in congestion using Congestion Driven Restructuring (CDR)**

## Improving Power While Achieving Aggressive Fmax Targets

In mobile applications, power is the most important consideration. With advanced-node FinFET technologies, dynamic power is the primary concern, although leakage still needs to be managed. Often, clock switching power can dominate, so CTS is a critical part of effective power management.

A technology that has helped with power and area reduction is Global Concurrent Clock and Data (CCD). Traditionally, placement optimization looked at the data-path only. It had no visibility into clocks and resulted in suboptimal solutions for power and area. Global CCD Optimization from IC Compiler II helped Samsung address these inefficiencies. This technology looks at both the clock and the data paths during the placement stage and feeds instructions to downstream engines, producing better optimizations. For example, Global CCD provides a better solution (right-hand side) by using available skew to delay the clock and meet timing without requiring expensive buffers (left-hand side).

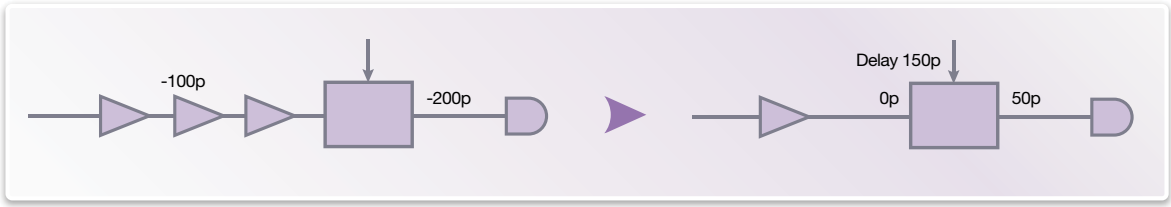


**Figure 5. Dynamic adjustment of useful skew during placement**

Samsung also benefited from CCD being used for more efficient clock-tree balancing. The standard approach is to balance all sinks, as shown on the left-hand side image below. In the right-hand side image, only sinks that are timing critical are balanced, making it possible to size-down buffers and use smaller flops in other sub-trees.

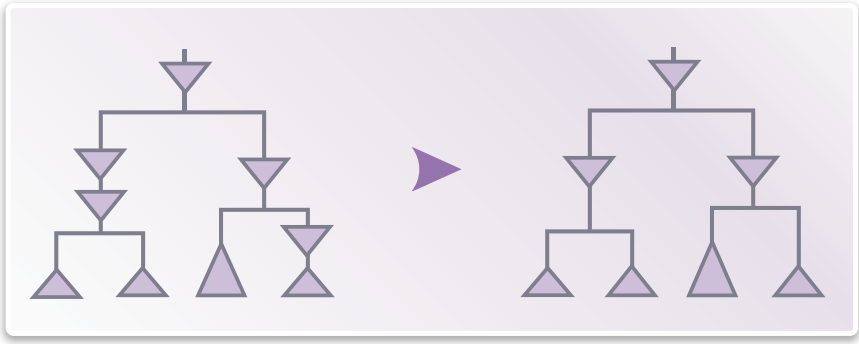

**Figure 6. Only sinks that are timing critical need to be balanced**

## Conclusion

Mobile Application Processors have stringent QoR targets, especially for power consumption. Moving to advanced-node FinFET technologies has many advantages, but also brings additional challenges for designers. IC Compiler II addresses the challenges of power-critical, advanced-node FinFET designs with many new technologies including POCV analysis, layer-promotion, GR-based CTS, CDR and Global CCD. These technologies continue to help Samsung meet their aggressive QoR and time-to-market targets.



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