SYNOPSYS®
Silicon to Software™

Optimizing QoR for Networking Applications with IC Compiler II

Along with other IC design leaders like Broadcom, Intel and Samsung, Mellanox participated in the 2016 IC Compiler II Technology Symposium in Santa Clara, CA. This is a brief recap of the Mellanox presentation.

Networking Applications: Bottlenecks and Solution

High-growth areas in the semiconductor industry include networking, storage infrastructure and data centers. As new, faster storage technologies have evolved, the bottleneck has shifted away from storage, and now the biggest issue is I/O bandwidth. Removing this obstacle requires a new way of designing interconnects. Speed is critical, but the path data takes through the interconnect can have a dramatic effect on performance. Mellanox Technologies' SoCs with intelligent interconnects increase data center efficiency by providing the highest throughput and lowest latency with fast data transfers.

Mellanox's product line includes switches, adapters and network processors. These designs have unique characteristics and challenges from an implementation standpoint. The "switch" designs, a backbone of networking applications, are used in many SoCs. In their presentation at the IC Compiler II Technology Symposium, Mellanox focused on physical implementation of "switch" designs in IC Compiler II.

Switch Design: Congestion Challenges Require a Well-Crafted Implementation Strategy

Design: In Mellanox's latest switch design, the complexity was multifaceted. The design targeting 16nm FF+ technology included 2M+ instances and had an intricate logic structure of over 50K highly interconnected I/Os. The logic level complexity was based on deep fan-in and fan-out cones, including thousands of start points and end points with large multiplexors (MUXes) and cyclic redundancy checker structures that had n-levels of XOR trees. These design characteristics led to high congestion near the ports and in the middle of the floorplan. This class of design presented Mellanox with a daunting challenge from both a congestion and design closure standpoint.

Complex MUX Structure: Figure 1 shows MUX trees with each tree depicted in a different color. The first level of MUXes is near the ports. Wires from the ports feed into large MUXes and cause major congestion near the ports. Some long wires, based on connectivity, intersect repeatedly while the next level of MUX tree has large buses that create congestion hot spots in the middle of the design.

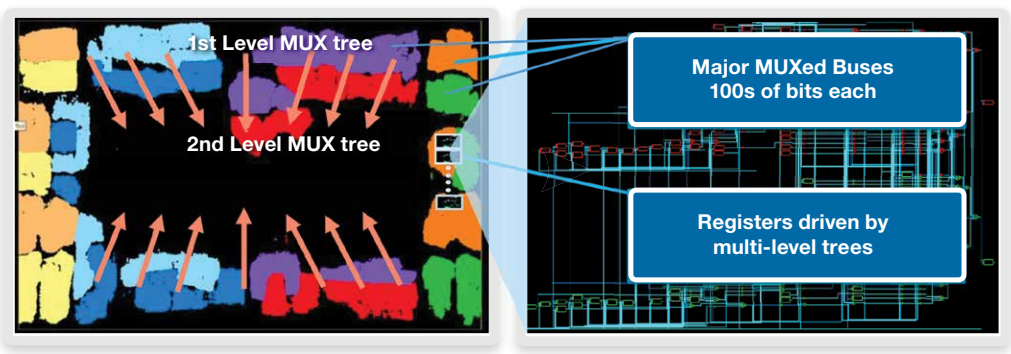

Figure 1. Complex MUX structure with large buses replicated 100s of times

Using a generic place-and-route flow, Mellanox observed heavy congestion near the ports and in the middle of their design with thousands of routing DRCs, poor QoR (timing, leakage, area), long runtimes and design closure issues. Based on these findings, Mellanox decided to use IC Compiler II to develop an automated implementation flow to meet their design objectives.

IC Compiler II's Congestion-Driven Restructuring (CDR)

Mellanox had a rich set of techniques at their disposal to address the design congestion and meet their QoR goals: applying keep-out margins on selective cells and placement blockages near high-density areas, adjusting global max-cell density and utilization, and congestion-driven restructuring. Among these techniques, congestion-driven restructuring provided the best results.

The CDR engine depicted in Figure 2, detects tangled designs and remaps and rewires the congested logic into smaller, localized logic cones.

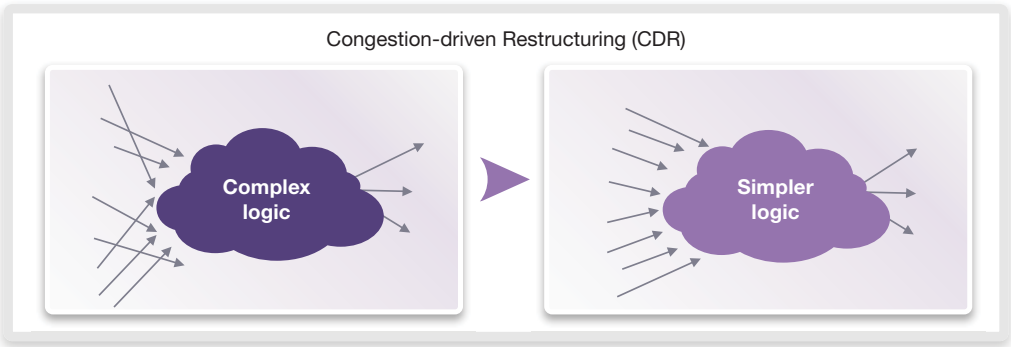

Figure 2. IC Compiler II CDR rewiring minimizes congestion

The four highlighted buffers shown in Figure 3 have long nets; CDR was able to shorten the wires and reduce crossings. The IC Compiler II CDR capability simplifies the large MUXes and remaps them to smaller local MUXes with fewer wires. CDR intelligently handles the complex logic structures and improves placement and routing while achieving the needed QoR.

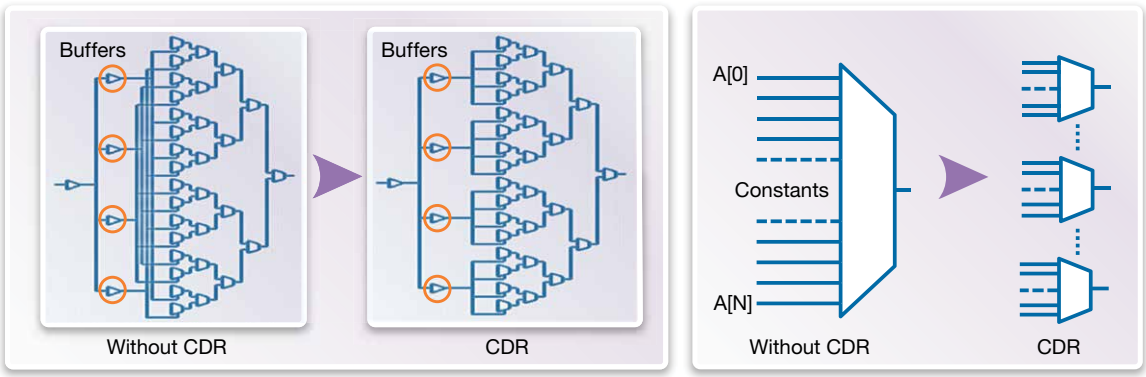

Figure 3. IC Compiler II CDR restructuring and placement improves routability and QoR

IC Compiler II's CDR-Based Flow

Mellanox leveraged the Synopsys Recommended Methodology (RM)-based flow, which includes the new CDR capability.

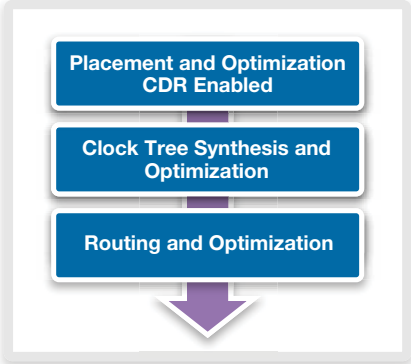

Figure 4. IC Compiler II CDR-based place-and-route flow

In the placement and optimization stage, Mellanox used the two-pass CDR-based flow. They defined soft keep-out margins on library cells with high pin density performing DRC and initial timing optimization, then ran incremental timing and congestion-driven placement followed by full placement and optimization. In the CTS and optimization step, Mellanox preserved the CDR transformations. Finally, they completed routing and enabled concurrent-clock-data (CCD) optimization in the post-route stage.

Results

IC Compiler II's CDR intelligently handled the complex structures, improved placement, routing and the overall design QoR.

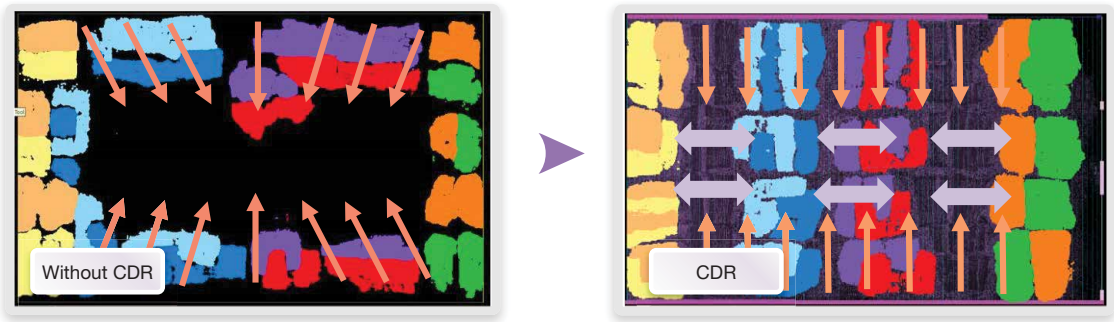

Figure 5. IC Compiler II CDR logic restructuring and intelligent net handling improved placement

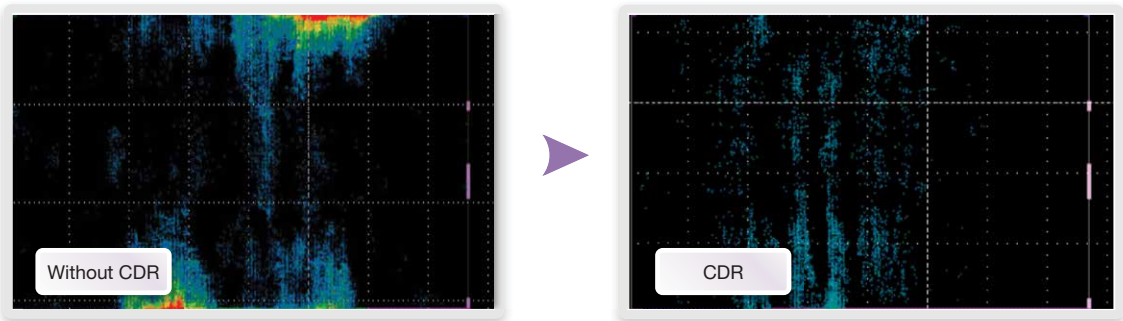

Figure 6. IC Compiler II CDR dramatically reduced the congestion and made the design routable

Conclusion

Using IC Compiler II's congestion-driven restructuring technology, Mellanox was able to achieve their power/performance/area QoR goals. Overall, using Synopsys' RM flow in tandem with CDR delivered a robust, portable and automated flow for implementing Mellanox's complex network SoCs.