

TetraMAX II

Next-Generation ATPG and Diagnostics Solution

Overview

TetraMAX® II is Synopsys' next-generation ATPG and diagnostics solution that lets design teams meet their test quality and cost goals with unprecedented speed. It delivers unparalleled runtime, ensuring patterns are ready when early silicon samples are available for testing. In addition, it generates significantly fewer patterns than existing solutions, allowing designers to reduce the time and cost of testing silicon parts, or increase test quality without impacting test cost. TetraMAX II is integrated with Synopsys' patented DFTMAX™ and DFTMAX Ultra, the leading test synthesis tools.

Key Benefits

- ▶ Generates high-coverage test patterns in hours instead of days
- ▶ Lowers test time and cost with fewer patterns than existing solutions
- ▶ Enables highly efficient utilization of hardware resources for ATPG and diagnostics
- ▶ Ensures easy, risk-free deployment into design and test flows
- ▶ Accelerates yield ramp by quickly isolating defect locations

Key Features

- ▶ Highly optimized, memory-efficient test generation, fault simulation, and diagnosis engines for order of magnitude faster ATPG runtime than TetraMAX and other commercial ATPG tools
- ▶ Fine-grained multithreading across multiple cores overcomes memory bottlenecks
- ▶ Identical test coverage and pattern reduction across different server configurations and machines for consistent analysis
- ▶ Production-proven rule checking, design modeling, and fault modeling for easy, risk-free deployment
- ▶ Physical diagnostics for accurate defect isolation
- ▶ Integration with Yield Explorer for rapid yield analysis

TetraMAX II ADV

- ▶ Advanced fault models for achieving extremely high test quality
 - Slack-based, cell-aware, static/dynamic bridging, path delay, hold-time, transition
 - Interfaces with PrimeTime®, StarRC™, and HSPICE® for easy access to physical and timing data used by the models
- ▶ IDDQ pattern generation and validation using VCS® for quiescent state testing
- ▶ Power-aware pattern generation for limiting power consumption during shift and capture

Unparalleled ATPG Runtime

Increasingly complex SoC designs and shrinking schedules require fast ATPG turnaround time. Even though compute servers have multiple cores available for pattern generation, the cores are often under-utilized because existing ATPG technologies require a large amount of memory per core, effectively limiting the actual number of cores.

TetraMAX II overcomes this memory bottleneck using new test generation and diagnosis engines (Figure 1) that are extremely fast, exceedingly memory-efficient, and highly optimized for fine-grained multithreading of ATPG and diagnosis processes across multiple cores. The core engines have been re-designed to surpass previous technologies that are limited by high memory usage, enabling TetraMAX II to achieve higher core utilization (Figure 2) and 10X faster runtime (Figure 3). Higher diagnostics throughput is achieved transparently, running multiple, faster simulations under the hood.

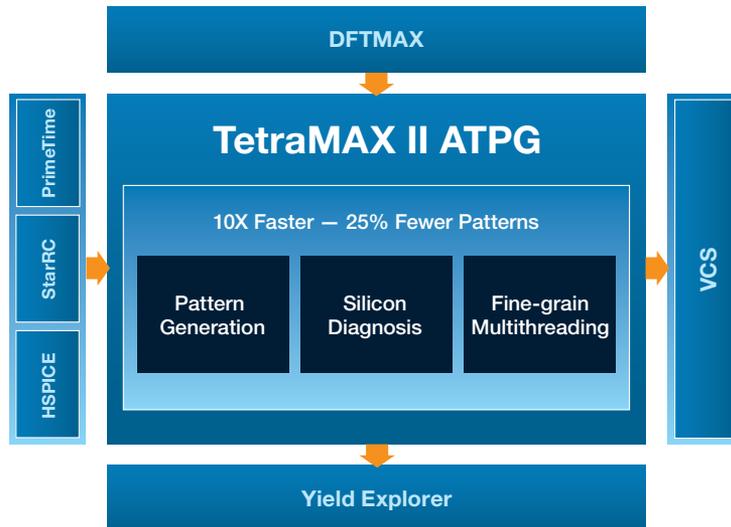


Figure 1. TetraMAX II is built on new engines to dramatically improve runtime and pattern count, while the rule checking, design and fault modeling infrastructure, and tool interfaces are unchanged

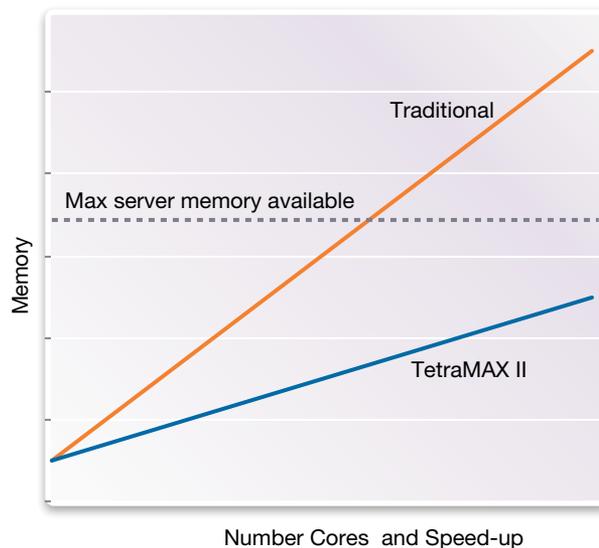


Figure 2. TetraMAX II eliminates memory bottlenecks and speeds-up ATPG as cores are added

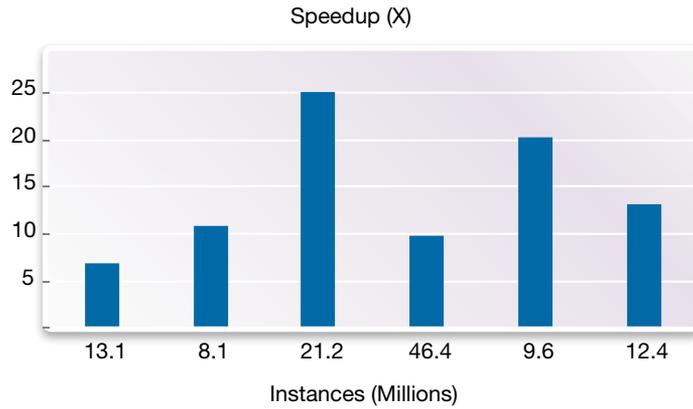


Figure 3. TetraMAX II runtime speedup compared to TetraMAX ATPG for different designs

25% Fewer Test Patterns

Decreasing pattern count reduces test time and cost or, depending on design requirements, facilitates an increase in test quality for the same cost. Algorithmic advances in TetraMAX II enable detection of more faults per pattern than existing methods, resulting in 25% fewer patterns on average (Figure 4). New multi-fault pattern optimizations also ensure that the default ATPG settings produce virtually the smallest pattern set. Moreover, TetraMAX II generates the identical compact pattern set bit-for-bit regardless of the number of cores used, facilitating easy QoR analysis and pattern debug across different server configurations and machines.

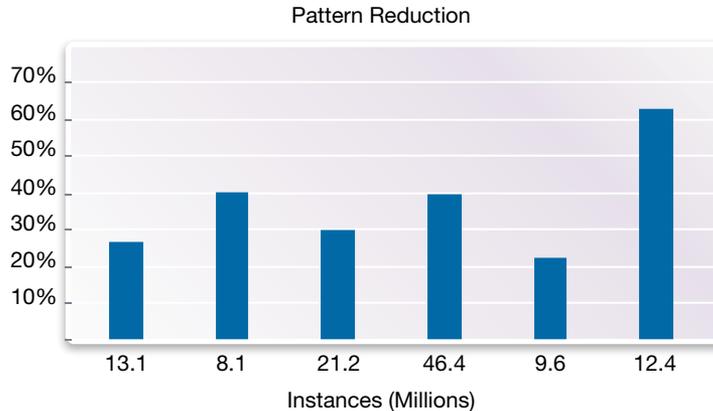


Figure 4. TetraMAX II pattern reduction compared to TetraMAX ATPG for different designs

Easy, Risk-Free Deployment

TetraMAX II is fully compatible with the existing TetraMAX product and supports the same production-proven capabilities, allowing designers to quickly deploy it risk-free on their most challenging designs. Although it is built on new engines to dramatically improve runtime and pattern count, the rule checking, design and fault modeling infrastructure, and tool interfaces are unchanged.

For example, TetraMAX II's design rule checker (DRC) supports full scan and partial scan test methodologies using mux-scan, clocked-scan, level sensitive scan design (LSSD), and proprietary schemes. For maximum flexibility, TetraMAX II accepts user-defined constraints and initialization patterns required for proper scan chain shifting. Complete support is provided for designs with IEEE 1149.1/6 internal scan shifting protocols and related techniques that minimize the number of external I/O pins required for ATPG.

Physical Diagnostics

Automatic and accurate defect isolation is an important step in diagnosing critical yield issues, both during production ramp as well as in volume manufacturing. In addition to identifying defective parts from manufacturing, TetraMAX II uses physical information about a design to quickly isolate the location

of defects in devices that fail ATPG patterns. It reads the test patterns and tester failure data, which are the differences between measured and expected responses to those test patterns, and reports the fault candidate locations that most likely explain the faulty device behavior observed on the tester. TetraMAX II uses advanced heuristics and a high-performance fault simulator for rapid and reliable results in a volume manufacturing environment.

To perform volume diagnostics and yield analysis, Yield Explorer directly reads diagnostics results from TetraMAX II and loads them into a complete database of previous diagnostics results, other test data, multiple domains of design data, and if available, process data from the fab. Yield Explorer then correlates the diagnostics results with specific failure mechanisms to determine the key design or systematic issues that are contributing to yield loss.

TetraMAX II ADV

TetraMAX II ADV offers additional functionality that includes advanced fault modeling, IDDQ testing, and power-aware pattern generation.

Advanced Fault Modeling

Many manufacturing defects will not be caught without additional high defect-coverage tests that specifically target subtle nanometer defects to further reduce defective parts per million (DPPM). TetraMAX II ADV utilizes advanced fault models such as slack-based, cell-aware, static bridging, dynamic bridging, path delay, hold-time, and transition to generate high defect-coverage test patterns. Some of these models use data generated by other Galaxy™ Design Platform tools (Table I). For example, cell-aware models leverage physical data from StarRC extraction and detailed timing information from HSPICE simulations for TetraMAX II ADV to target timing-critical defects inside cells.

Fault Model	Galaxy Design Platform Tool
Bridging	StarRC
Path delay	PrimeTime
Hold-time	PrimeTime
Slack-based	PrimeTime
Cell-aware	StarRC, HSPICE

Table 1. ATPG fault models and the tools that create physical or timing data for the models

IDDQ Testing

TetraMAX II ADV generates a minimal set of high fault coverage patterns for IDDQ testing purposes, and constrains the test patterns to avoid excessive current during the quiescent state. It then accurately validates these patterns for low quiescence using Synopsys VCS or other Verilog simulator, thereby ensuring the IDDQ patterns will function on the ATE.

Power-Aware ATPG

Scan testing typically increases transistor switching activity by many times their peak functional-mode levels, leading to excessive power consumption. Too much power consumption during test can lead to the failure of good devices on the tester and unnecessary yield loss. TetraMAX II ADV limits power consumption during scan and capture by automatically reducing switching activity to levels consistent with normal operation, based on designer-specified power budgets. Power reduction is achieved without compromising test coverage.

TetraMAX II ADV also supports hardware-assisted shift power reduction, which decreases average shift power and pattern count compared to an ATPG-only approach through the use of independently controlled scan chain groups implemented in DFTMAX or DFTMAX Ultra.

Tight Links With Synopsys Tools

TetraMAX II utilizes established interfaces with Galaxy Design Platform tools and other Synopsys tools to deliver the highest quality test and the fastest, most productive flows:

- ▶ Integrated with DFTMAX and DFTMAX Ultra, which are built into Design Compiler® RTL synthesis to optimize timing, power, area, and congestion for test as well as functional logic
- ▶ Integrated with Yield Explorer for seamless volume diagnostics and yield analysis to uncover design and process issues causing yield loss
- ▶ TetraMAX II ADV is guided by slack data from PrimeTime to accurately target timing-critical defects
- ▶ TetraMAX II ADV leverages physical data from StarRC extraction and detailed timing information from HSPICE simulations for cell-aware ATPG that targets timing-critical defects inside cells

Netlist and Test Pattern Formats

TetraMAX II supports the same industry standards for data formats, simulation testbenches, and tester interfaces:

- ▶ Circuit netlist: Verilog, VHDL (1987 and 1993)
- ▶ Library: Verilog functional (Structural and UDPs)
- ▶ Timing exceptions: Synopsys Design Constraints (SDC)
- ▶ Design layout: LEF/DEF interface
- ▶ Simulation testbench: Verilog (serial and parallel)
- ▶ Test Patterns: STIL, WGL, Verilog
- ▶ Tester fails: STDF (V4 and V4-2007)

For more information about Synopsys products, support services, or training, visit us on the web at: www.synopsys.com , contact your local sales representative, or call 650.584.5000.