SYNOPSYS®
Silicon to Software™

Synplify Pro and Premier

Fast, Reliable FPGA Implementation and Debug

Overview

The Synopsys FPGA design tools are comprised of synthesis and debug tools that enable designers to quickly deliver competitive products to market with the lowest schedule risk.

The Synplify synthesis tools provide fast runtime, performance, area optimization for cost and power reduction, multi-FPGA vendor support, incremental and team-design capabilities for faster FPGA design development.

In addition, Synplify supports DesignWare® IP integration, links to VCS® high-performance functional verification, integration with Identify RTL Debugger, and an ASIC compatible synthesis flow.

Benefits

- Fast time to market for FPGA-based products with support of IP reuse, single pass debug flow
- Flexible FPGA support through multi-vendor synthesis and debug retargeting from a single RTL source
- Advanced design for high reliability features including TMR, safe and fault-tolerant FSM implementations and ECC RAM inference
- Accurate timing correlation improves timing closure
- Automation of FPGA-based prototyping including clock conversion, memory substitution, UPF and DesignWare IP support
- Synthesis support for leading node and legacy FPGA devices supporting long product lifetimes

Key Features

- Industry leading FPGA synthesis technology
- Best quality of results (QoR) for timing performance and area/cost reduction
- TCL-based scripting environment for control and automation
- Industry standard Synopsys Design Constraints (SDC) support for timing requirements
- Automation of high reliability design techniques for SEU migration
- Multi-processing/multi-threading for faster runtimes with smaller memory footprints
- Broad language support for Verilog, VHDL, VHDL-2008 and SystemVerilog
- RTL debugging for simulator-like visibility into FPGA hardware
- Direct support for DesignWare® IP
- Simulation projects export into Synopsys VCS environment
- Direct support for IEEE P1735 encrypted IP

Market Trend and Customer Challenges

There is an increasing use of programmable chips thanks to the rise in capacity and reduction in power at each process node. Designers are now experiencing some tough new challenges. For example, 28nm FPGAs have the equivalent capacity of 50 million ASIC gates and this drives a need for more powerful synthesis tools. Synplify synthesis tools provide designers with methodologies that deliver automation, faster turnaround times, more predictable timing closure, design for high reliability, power management, advanced verification techniques and the integration of IP from many sources. The Synplify toolset automates many functions so that designers can focus on their own product differentiation, while meeting schedule and cost targets.

Designing Products With FPGAs

Customers designing end products with FPGAs are challenged with meeting the proper balance of cost, performance and power while managing risk and delivering on time within budget. Synplify tools help to stay ahead of the competition by providing customers with fast hardware system bring-up, at the best system performance and cost to enable the software development sooner. Synplify delivers rapid runtimes using incremental synthesis flows, fast synthesis mode and automated block-based design. Automatic compile point technology can automatically boost synthesis runtimes by leveraging multiple processors.

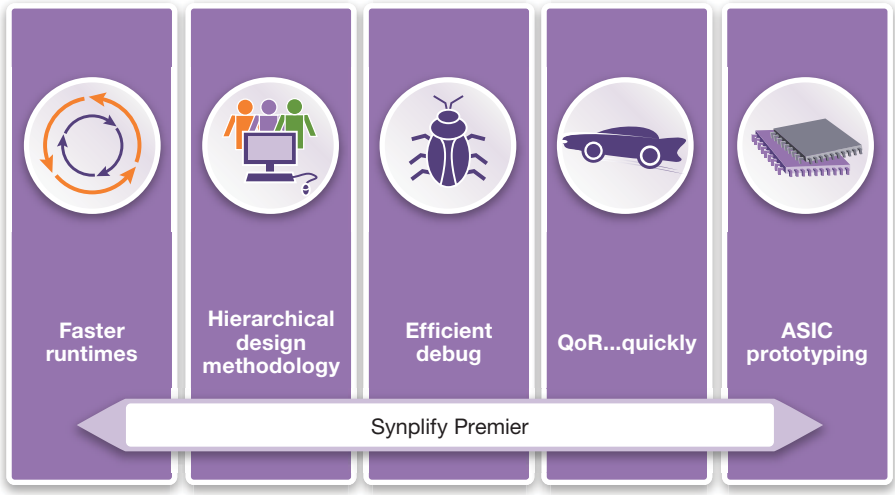

Figure 1: Synplify Premier

Debug Where You Design, In RTL

The Synplify software includes the Identify RTL Instrumentor to provide an easy-to-use method for finding functional errors in FPGA designs that are operating on the board. The solution offers simulator-like visibility into the implemented FPGA hardware. Using the Identify Instrumentor tool, users can annotate in the RTL the signals and conditions that need to be monitored directly. Nodes, which may be used as breakpoints and watch points, are displayed for easy menu-driven instrumentation. The user can then run synthesis and placement and routing to implement the FPGA with associated monitoring logic. Once the FPGA has been programmed, the Identify RTL Debugger is run, allowing designers to view actual signal values from an operating FPGA, directly superimposed on RTL code. In this way, users can perform in-system debug at the target operating speed.

Broad RTL Language Support

Taking advantage of the latest HDL developments, such as System Verilog and VHDL-2008, provides an advantage in engineering productivity. Less time spent coding RTL means more time for design architecture exploration and developing product differentiation. Mixed-language support has become the standard for many FPGA designers as IP from various sources is incorporated into today's designs. For FPGA prototypers, the Synplify Premier tool's language support encompasses VHDL, VHDL-2008, SystemVerilog, and Verilog and is compatible with Synopsys' Design Compiler ASIC synthesis products. Advanced features such as Verilog Cross Module References are provided. System Verilog Assertions are parsed and ignored, allowing designers to synthesize and verify designs from the RTL source.

Design for High Reliability

Synplify Premier includes features that automate the creation of highly reliable designs such as those used in medical, automotive, industrial automation, communications, military and aerospace applications. These high reliability capabilities are useful for implementing DO-254 compliance and include:

- Safe Finite State Machines (FSMs) implementation options including Hamming-3 error-detection and correction
- Triple Modular Redundancy (TMR) with voting logic
- Duplicate with compare circuitry creation for error detection and monitoring, and to trigger, for example, scrubbing
- Controls to limit synthesis optimizations, allowing designers to maintain critical logic and nodes within the design
- Inference of Error Correcting RAMs and TMR of RAMS
- Highly customizable design reporting to enable area/timing vs. reliability trade-off decisions, design process checks, and design documentation
- Design analysis at the RTL and netlist level using HDL Analyst
- FPGA debug on the board using the Identify RTL Debugger
- Repeatable synthesis results and netlist naming conventions from one synthesis run to the next

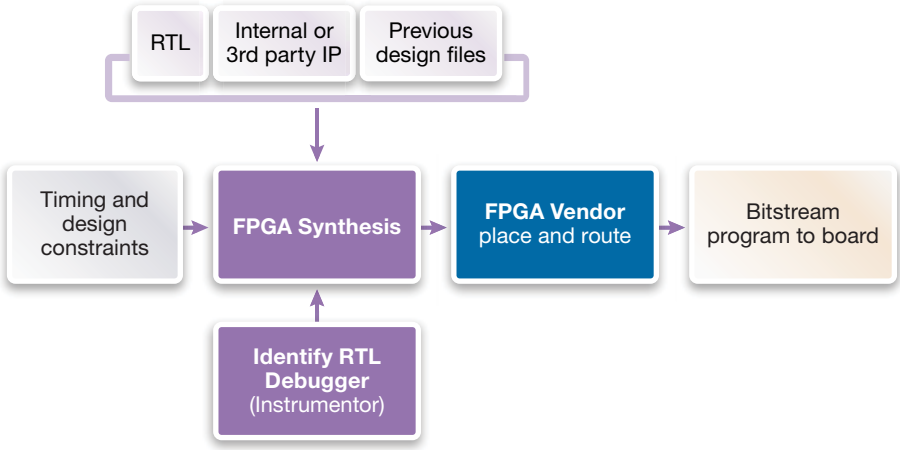

Figure 2: FPGA Design Flows must Understand IP from Many Sources

ASIC Prototyping Automation

Synplify software uniquely delivers RTL compatibility between FPGA and ASIC flows allowing designers to synthesize the same ASIC RTL source files into an FPGA. The built-in gated-clock conversion capability and full integration with the DesignWare Library's Datapath and Building Block IP means that the DesignWare components used in ASIC and FPGA flows are completely synchronized, ensuring flow compatibility and accurate verification.

Synplify Premier automates the process of implementing your ASIC / SoC in an FPGA-based prototype, from the same source RTL files. ASICs have fundamentally different architectures from FPGAs, leading to the need to convert clock architectures, exclude or substitute memories, and exclude or insert test logic. The ability to read and synthesize ASIC IP, such as Synopsys DesignWare IP, is also required. The Synplify toolset automates this process, allowing you to directly synthesize and convert the latest version of your ASIC files into an FPGA-based prototype.

Industry-Leading Quality of Results Including DSP-Aware Synthesis

The Synplify products include advanced logic synthesis algorithms that provide the best logic synthesis timing and quality of results in the industry. The synthesis software performs both high-level optimizations as well as detailed optimizations tailored to the specific FPGA architecture and its resources. It automatically infers many DSP and memory functions from RTL code and has DSP-aware mapping technology and automatic memory inferencing to take full advantage of each FPGA's unique memory, register and DSP resources. The Synplify Premier product is designed to accept optimized RTL output from the Synphony Model Compiler high-level synthesis tool, allowing broad design exploration and faster implementation of DSP and datapath-oriented functions being implemented in FPGAs.

For more information on the Synopsys FPGA design solution visit www.synopsys.com/FPGA.

Synplify Features	Synplify Pro	Synplify Premier
Integration with FPGA vendor place and route system tools	✔	✔
TCL-based scripting environment for control and automation	✔	✔
Customized mapping per FPGA family ensures optimal implementation and technology independence	✔	✔
Automatic memory and DSP inferencing provides optimal area, power and timing quality of results	✔	✔
Timing knowledge of Altera and Xilinx modules enables system-level optimizations	✔	✔
FSM extraction, optimization and debug, with user control	✔	✔
Best quality of results (QoR) for timing performance and area/cost reduction	✔	✔
Automatic compile points for incremental flow, delivering up to 4x faster runtime while maintaining QoR	✔	✔
Broad language support with VHDL, Verilog, SystemVerilog, VHDL-2008 and mixed language synthesis	✔	✔
Advanced design debug and diagnosis through HDL Analyst and hierarchical debug flows	✔	✔
Automated gated clock conversion for FPGA-based prototyping support		✔
Integrated Identify RTL Debugger to quickly find functional errors		✔
Automated design for high reliability and safety-critical design including DO-254		✔
Integration with VCS Simulator		✔
Direct support for DesignWare IP		✔

SYNOPSYS®
Silicon to Software™

Synopsys, Inc. • 690 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

08/15.RD.CS5374.