SYNOPSYS®
Silicon to Software™

StarRC
Parasitic Extraction

Overview

StarRC™ is the EDA industry's gold standard for parasitic extraction. A key component of Synopsys' Galaxy™ Design Platform, it provides a silicon-accurate and high-performance extraction solution for SoC, custom digital, analog/mixed-signal and memory IC designs. StarRC offers modeling of physical effects for advanced process technologies, including FinFET technologies at 16nm, 14nm, 10nm, 7nm, and beyond. Its seamless integration with industry standard digital and custom implementation systems, timing, signal integrity, power, physical verification and circuit simulation flows delivers unmatched ease-of-use and productivity to speed design closure and signoff verification.

StarRC Solution

Semiconductor process technology has been continually scaling down for the past four decades and the trend continues. Shrinking process geometries, combined with the use of new device structures like FinFETs and an increasing number of metal layers at each new process node, are introducing millions of new parasitic effects in designs. In addition, soaring design sizes and complexities are increasing the sensitivity of circuits to parasitics due to the increasing impact on signal timing, noise and power. To ensure a successful silicon design and meet tapeout schedules, IC designers need an advanced parasitic extraction solution that delivers signoff accuracy and increased designer productivity. Furthermore, they need a solution that is versatile enough to manage the full design spectrum from custom digital, analog/mixed-signal (AMS) to full-chip memory and SoC designs.

Synopsys' StarRC is the proven high-accuracy and high-performance parasitic extraction solution for digital and custom IC implementation and signoff verification (Figure 1). Trusted by hundreds of semiconductor companies and used in thousands of production designs, StarRC provides sub-femtofarad-accurate technology for design at advanced process technologies. It achieves its high accuracy by performing detailed modeling of device and interconnect parasitic effects in nanometer process technologies. The advanced modeling and accuracy is complemented with the embedded Rapid3D field solver technology for circuits that require even higher accuracy.

StarRC delivers industry-leading performance and capacity for users' gate-level and transistor-level extraction needs. StarRC's multi-core distributed processing technology delivers excellent scalability for efficient utilization of available hardware, and its simultaneous multi-corner extraction (SMC) feature allows the increasing number of extraction corners required for analysis to be processed within a single run with significantly reduced runtime and disk usage. Its seamless integration with Synopsys' place-and-route IC Compiler™ and IC Compiler II physical implementation, gold standard PrimeTime® static timing analysis (STA) signoff, Galaxy Custom Designer® mixed-signal implementation, IC Validator physical verification, CustomSim™ circuit simulation and other third-party implementation and signoff tools enables users to significantly accelerate their design implementation and verification.
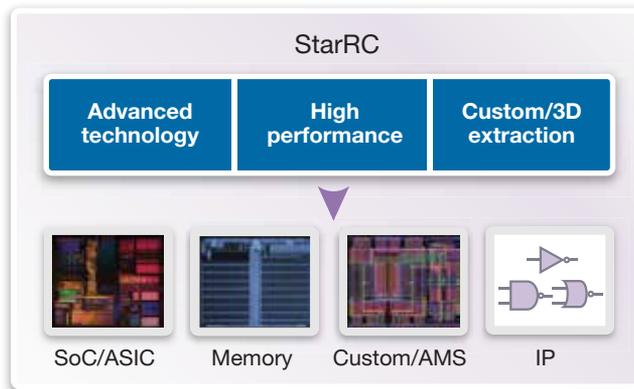
Figure 1: StarRC provides a parasitic extraction solution for gate-level and transistor-level digital and custom IC designs

Benefits

▶ Foundry gold standard for extraction accuracy with broadest qualification and adoption

▶ Leader in advanced modeling, including FinFET and color-aware multi-patterning at 10nm/7nm and beyond.

▶ High performance and capacity for gate and transistor-level extraction, enabled by multi-core distributed processing and simultaneous multi-corner extraction

▶ Tightly integrated with industry leading IC Compiler II and PrimeTime solutions for faster full-flow ECO turn-around time

▶ Unified Rapid3D fast field solver for critical net, IP, and custom circuit extraction

▶ Advanced netlist reduction features for faster simulation turn-around time

▶ Inductance extraction for high frequency digital RLC clock net analysis

▶ 3D-IC extraction solution for interposer and stacked die technologies

▶ Integration with IC Validator physical verification, CustomSim circuit simulation, Galaxy Custom Designer and other third party implementation and custom design solutions for increased designer productivity

Advanced Process Modeling

Increasing process variation and new parasitic effects introduced at each new technology node are significantly increasing design challenges. Process technologies at 40nm and 28nm elevated a variety of physical effects once considered secondary to primary factors affecting circuit behavior, risking performance degradation, silicon failure and lower yields if not accurately modeled. Some typical process modeling capabilities offered by StarRC include litho-aware extraction and chemical-mechanical polishing (CMP)-based thickness variation extraction, as well as modeling of micro-loading effects and low K dielectric damage. For transistor-level circuit modeling, gate-to-contact capacitance, gate-to-diffusion capacitance, and contact etch effects are some of the device parasitics which are accurately modeled by StarRC for increased signoff integrity, with the additional benefit of being modeled in context with the layout environment for even higher accuracy.

In addition, striking changes in process technology, like double-patterning lithography at 20nm, 16nm/14nm FinFET transistor architecture, 10nm/7nm multi-patterning lithography, and further FinFET architecture enhancements at 10nm

and 7nm are requiring consideration of a host of completely new and complex effects with even more ramifications on extraction, timing analysis and design robustness. More than ever, the accuracy of parasitic modeling and extraction results is contributing to overall design integrity.

20nm Double Patterning Technology (DPT) Modeling

At 20nm, significant capacitance variation is introduced by double-patterning, a fabrication strategy where metal lines on a single layer are created in two separate masking steps to achieve finer metal pitch. Misalignment between the patterns causes coupling capacitance between adjacent metal lines to increase in one direction and to decrease in another (Figure 2a). StarRC models these capacitance variations with a novel modeling technique that ensures that these effects are accounted for accurately while preserving the existing signoff flows.

FinFET Modeling

Even more radical changes are introduced by 16nm/14nm FinFET transistor architecture. In contrast with planar transistors, FinFETs are able to achieve better control over the source-drain channel because the gate encloses the channel on three sides, resulting in higher mobility, greater drive strength, lower switching currents and lower leakage currents. But this multi-gate, non-planar architecture also introduces more complex co-vertical geometries and many new capacitive elements that must be accurately extracted due to their impact on circuit performance. StarRC uses a uniquely detailed FinFET physical profile derived from QuickCap®'s field solver technology for 3D modeling of layout-dependent middle-end-of-line (MEOL) parasitic effects (Figure 2b) for increased accuracy. At 10nm and 7nm, new materials and geometries are being introduced to FinFETs to reduce operating voltage while improving transistor performance. Due to its advanced modeling solution, StarRC is the extraction tool of choice for foundries and IP developers to model new parasitic effects and ensure proper characterization of FinFET devices.

10nm/7nm Multi-patterning Modeling

At 10nm and 7nm, where even finer metal pitch geometries must be resolved than at 20nm, multi-patterning of three or more mask layers is used. This requires an even more complex capacitance variation model which requires properly identifying each conductor's printed mask layer, or "color", as well as accounting for adjacent metal line width and spacing effects (Figure 2c). StarRC's 10nm and 7nm extraction solutions are fully color-aware and include updated Interconnect Technology Format (ITF) constructs to support all etch effects associated with a range of foundry multi-patterning lithography strategies for 10nm and 7nm.
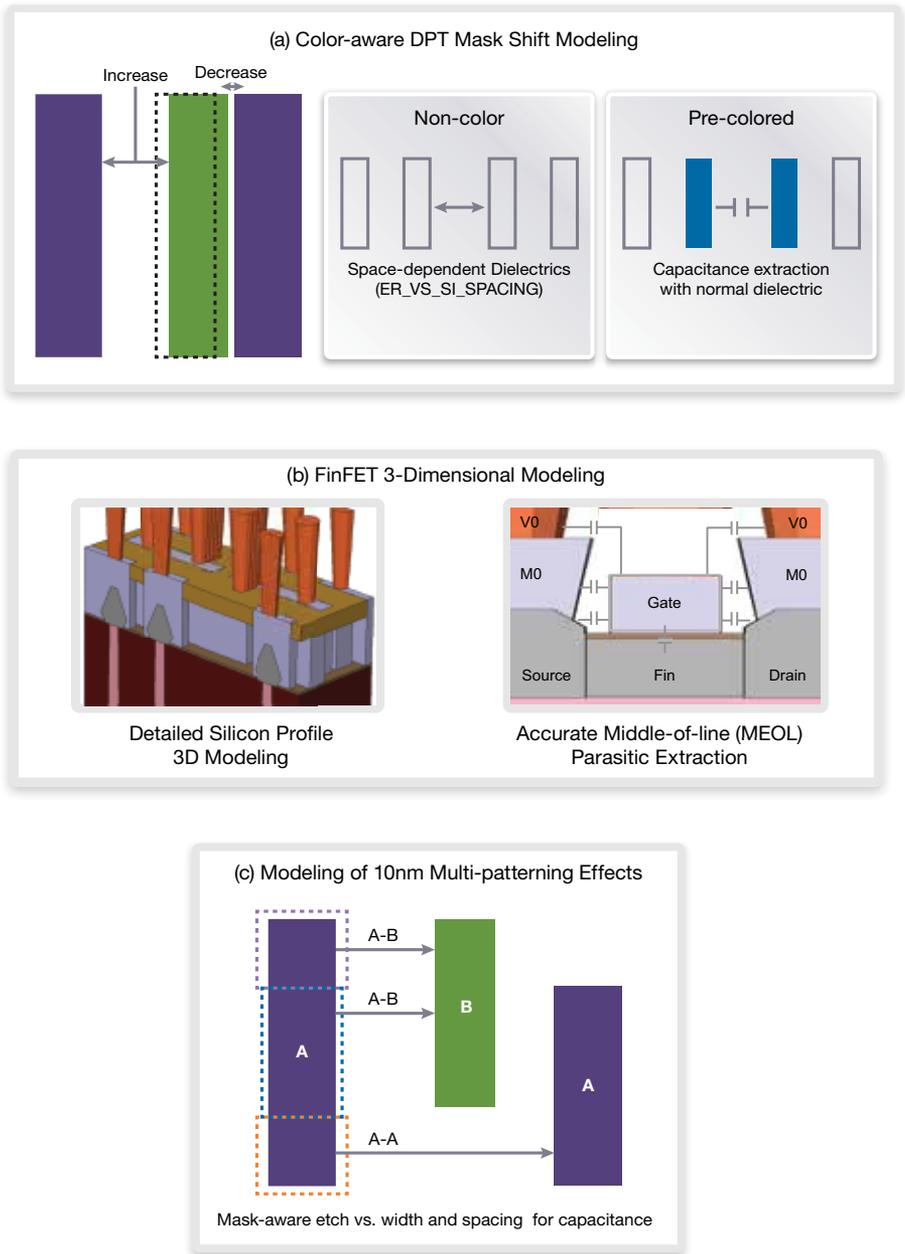

(a) Color-aware DPT Mask Shift Modeling

Increase   Decrease

Non-color
Space-dependent Dielectrics
(ER_VS_SI_SPACING)

Pre-colored
Capacitance extraction
with normal dielectric

(b) FinFET 3-Dimensional Modeling

Detailed Silicon Profile
3D Modeling

Accurate Middle-of-line (MEOL)
Parasitic Extraction

V0   M0   Gate   M0   V0
Source   Fin   Drain

(c) Modeling of 10nm Multi-patterning Effects

A-B
A-B
A-A
A   B   A

Mask-aware etch vs. width and spacing for capacitance

Figure 2: StarRC's advanced 20nm DPT, 16nm/14nm FinFET, and 10nm modeling for signoff accuracy

3D-IC Modeling

StarRC also supports extraction for stacked die and silicon interposer 3D-IC technologies (Figure 3). StarRC extracts through-silicon vias (TSV) and substrates, TSV-TSV capacitive coupling, silicon interposers, micro-bump structures, and routing layers on each die. StarRC supports modeling substrates as either floating or grounded. StarRC's extraction and modeling of through-silicon vias and substrates through Synopsys' Interconnect Technology Format (ITF) has been qualified by several major foundries and is found in their 3D-IC reference flows.

Multi-Core Distributed Processing

Multi-core processor hardware has become common due to the widespread need for higher productivity. A large majority of design jobs are run on compute farms consisting of multi-core machines, and IC designers seek design tools that harness the full potential of their hardware network. StarRC's multi-core technology works seamlessly with popular commercial grid computing management software to maximize efficiency across multi-core processors, as well as multi-processor compute farms, to take full advantage of available hardware. StarRC offers high performance per CPU core, with 12X scalability on 16 cores and over 20X on 32 cores. In addition, StarRC multi-core distributed processing provides easy-to-setup compute resource allocation, automated design partitioning to multiple cores, balanced load sharing, and automatic failure recovery for a superior fault-tolerant server environment.

Simultaneous Multi-Corner Extraction

The increase in process variation and decrease in process geometries found in technology nodes at 20nm and below have resulted in a significant growth in the number of extraction corners requiring analysis. This in turn is having a significant impact on the efficiency of designers. To mitigate the increased turnaround time (TAT) caused by this rise in extraction corners, StarRC offers ultra-scalable simultaneous multi-corner extraction,
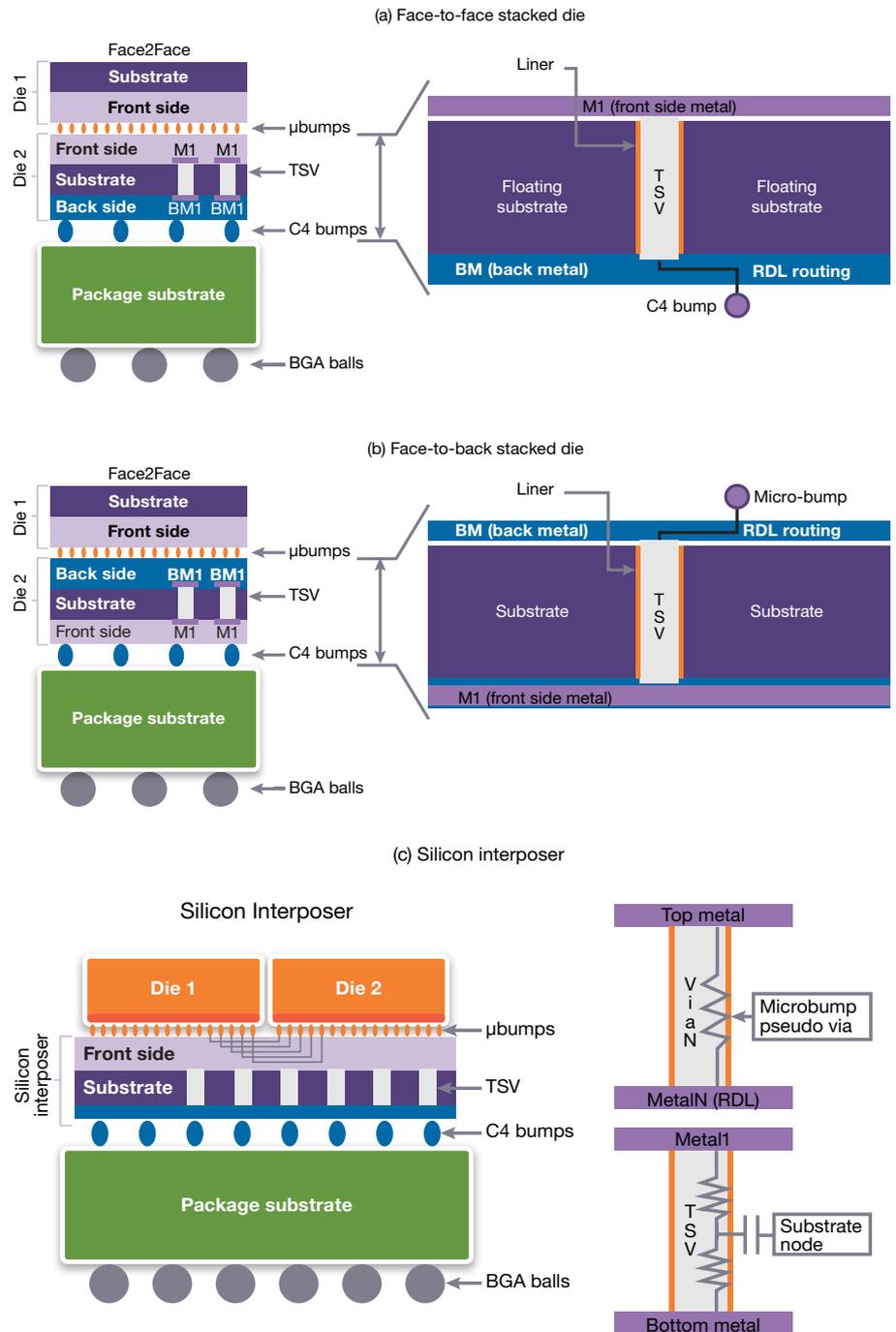

Figure 3: 3D-IC stacked die and interposer profiles example

wherein all extraction corners can be analyzed within a single run. For designers traditionally executing multiple extraction runs in parallel, runtime speedup of up to 3X is achieved when using SMC and aggregating hardware resources within a single run. Those with resource–limited environments running serial extractions will see even greater TAT benefits when comparing total extraction runtime to a single SMC run. Runtime speedup of 2-3X can be seen across designs ranging in size from 2M to 300M instances. StarRC's ultra-scalable multi-core technology enables the use of over 100 CPU cores for faster speedup on large designs. Disk usage with SMC is also significantly reduced, typically by 75% or more depending upon the number of corners extracted. StarRC's SMC feature is available for both gate-level and transistor-level extraction.

Fast ECO Extraction

The ECO timing closure cycle has become a significant TAT issue for designers. Final design optimization which may affect only a small portion of a chip introduces lengthy delays in tapeout schedules. In order to minimize the impact of these changes in extraction, StarRC fast ECO extraction allows designers to extract only those nets affected by ECO changes versus re-analyzing an entire design. StarRC fast ECO extraction achieves up to 5X faster extraction TAT while maintaining the same signoff accuracy as full extraction. StarRC is also tightly integrated with PrimeTime STA and IC Compiler II place and route solutions, allowing designers to achieve faster ECO turn-around time across their entire digital implementation and signoff flow. IC Compiler II directly updates StarRC with ECO database changes for faster identification of ECO affected nets. PrimeTime also directly reads Galaxy Parasitic Data (GPD) from StarRC, eliminating the need for separate SPEF netlists to be generated by StarRC and input into PrimeTime.

Inductance Extraction for High Frequency Clock Nets

Inductance effects are becoming increasingly important to model for high frequency, low resistance nets, such as those for high-performance clocks routed on upper layer metals. Inductance effects on clock nets include steeper edge rates, push out delays, and voltage undershoot and overshoot. StarRC's inductance extraction feature models the inductance on clock nets with pre-defined power/ground net shielding and includes the inductance values in Detailed Standard Parasitic Format (DSPF) netlists for simulation analysis. Inductance extraction is invoked from the same StarRC interface as RC extraction and uses standard foundry technology files for input. The inductance values extracted with this feature correlate within 10% to FastHenry, ensuring high accuracy as well as high productivity.
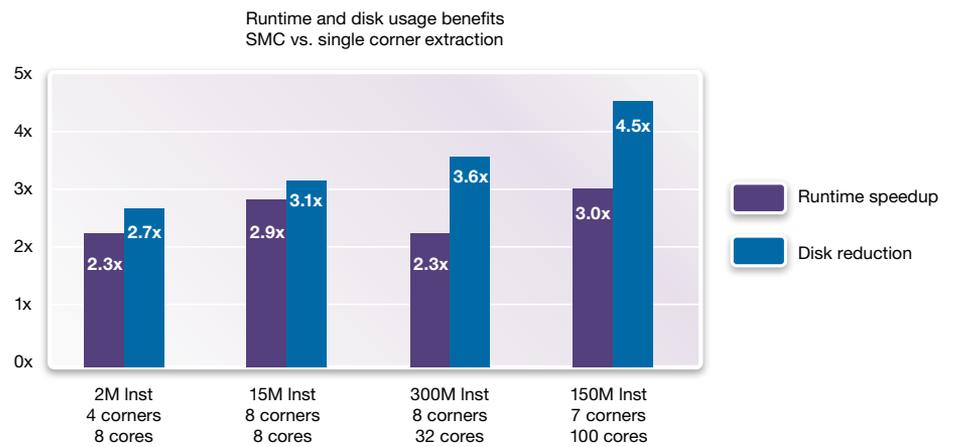

Runtime and disk usage benefits
SMC vs. single corner extraction

Figure 4: Design TAT and Disk Usage Improvement with SMC

High Accuracy Fast Field Solver Extraction

For timing sensitive implementations such as clock networks, memories, analog/mixed signal/RF, high-speed digital, standard cells and other IP designs, accuracy is a non-negotiable design criterion. Designers of such critical IP and circuits generally require field solver level accuracy as well as fast turnaround time. StarRC offers integrated fast field solver extraction, Rapid3D with merged QuickCap NX technology, for industry's highest accuracy 3D extraction. It incorporates the latest advancements in field solver algorithms to deliver highest performing 3D extraction while providing golden accuracy. The embedded Rapid3D technology complements StarRC's primary extraction engine for 3-dimensional self- and coupling-capacitance extraction of critical circuits. Within the single StarRC environment, users can supply a list of nets that need the highest level of accuracy for capacitance extraction. The tool not only extracts the nets in the regular flow, but it also creates a subset of the design based on the user-specified nets to be extracted using the field solver technology. A merged netlist is generated including the higher accuracy field solver extracted nets (Figure 5).

CustomSim Circuit Simulator Integration

Post-layout simulation runtimes are increasing 2-4X with every new process generation. More accurate and efficient parasitic extraction is needed to accelerate simulation and meet tapeout schedules. StarRC offers seamless integration with Synopsys' CustomSim circuit simulator and a wide range of innovative features to boost simulation performance and capacity while preserving signoff accuracy. StarRC's exclusive interface with CustomSim includes active node extraction, post-layout acceleration with hierarchical back-annotation, and power network optimization. The integration between the two tools enables over 10X simulation performance speed-up for custom IC and memory designs.

Custom AMS Design Platform Integration

StarRC is integrated with Synopsys' Galaxy Custom Designer mixed-signal implementation system and with Cadence®'s Virtuoso® Analog Design Environment (ADE) for custom AMS and custom digital designs. StarRC and Galaxy Custom Designer offer users the unique benefits of an OpenAccess interface combined with the ease-of-use of the familiar Synopsys implementation environment using a common data flow. For the Virtuoso environment, StarRC generates OpenAccess or Cadence DFII database parasitic views for netlisting and simulation, compatible with common netlisting interfaces used within ADE. StarRC offers full parasitic probing capabilities within the parasitic view or within the matching schematic view (Figure 6). The parasitic prober allows users to interactively observe point-to-point resistance, total net capacitance, net-to-net coupling capacitance and cross-probing between schematic and parasitic views. It also provides the ability to output probed parasitics to an ASCII report file, and to annotate parasitic view total capacitance values to an associated schematic view.

Process Modeling

- 10nm/7nm color-aware multi-patterning
- Via coverage resistance variation modeling
- FinFET 3D modeling
- Color-aware double patterning
- Trench contact modeling
- Inductance extraction for high frequency clock nets
- Embedded 3D field solver
- 3D-IC, Silicon Interposer TSV modeling
- Via etch modeling
- Width- and spacing-dependent thickness variation
- Density-based thickness variation
- Width- and spacing-dependent resistance per square (RPSQ) variation
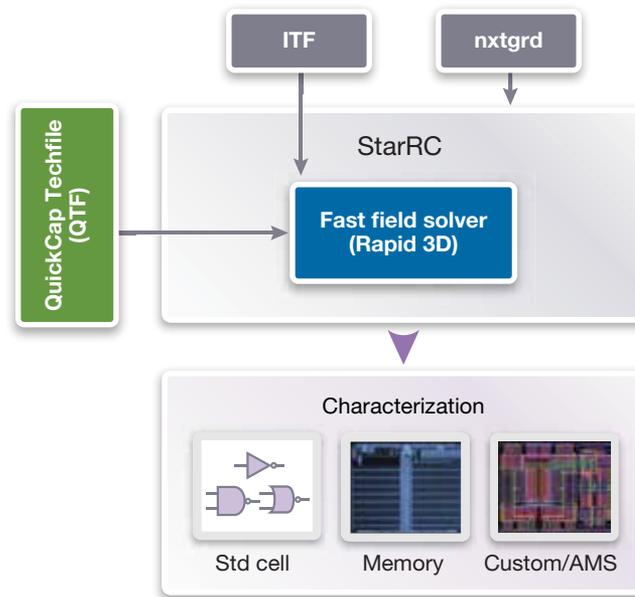
StarRC FS flow
(QuickCap Inside)

Figure 5: StarRC integrated fast field solver extraction offers high-accuracy extraction for critical IP within a single extraction environment

- RPSQ variation as function of silicon width
- Nonlinear RPSQ variation
- Trapezoidal polygon support
- Copper interconnect, local interconnect modeling
- Low-K dielectric, silicon on insulator (SOI) modeling
- Conformal dielectric process support
- Via cap extraction
- Layer etch effects
- Temperature-dependent resistance modeling for conducting layers and vias
- Support of background dielectric
- Nonlinear via resistance modeling
- 45 degree routing support
- Support of multiple inter-layer and intra-layer dielectric
- Support for co-vertical conductors
- Support for non-planarized metal

Productivity and Ease-of-use

- Multi-core distributed processing
- Simultaneous multi-corner extraction
- Fast ECO extraction for ECO TAT reduction
- Clock inductance extraction
- Integration with PrimeTime and IC Compiler II for ECO TAT reduction
- CustomSim circuit simulation integration
- Custom layout environment integration
- Physical implementation interface (GDSII, Milkyway™, LEF/DEF, NDM)
- Galaxy Parasitic Data (GPD) interface to PrimeTime
- Metal fill re-use for ECO TAT reduction
- Hierarchical layout-versus-schematic (LVS) and advanced device parameter ADP extraction flow
- Active node extraction

Schematic view

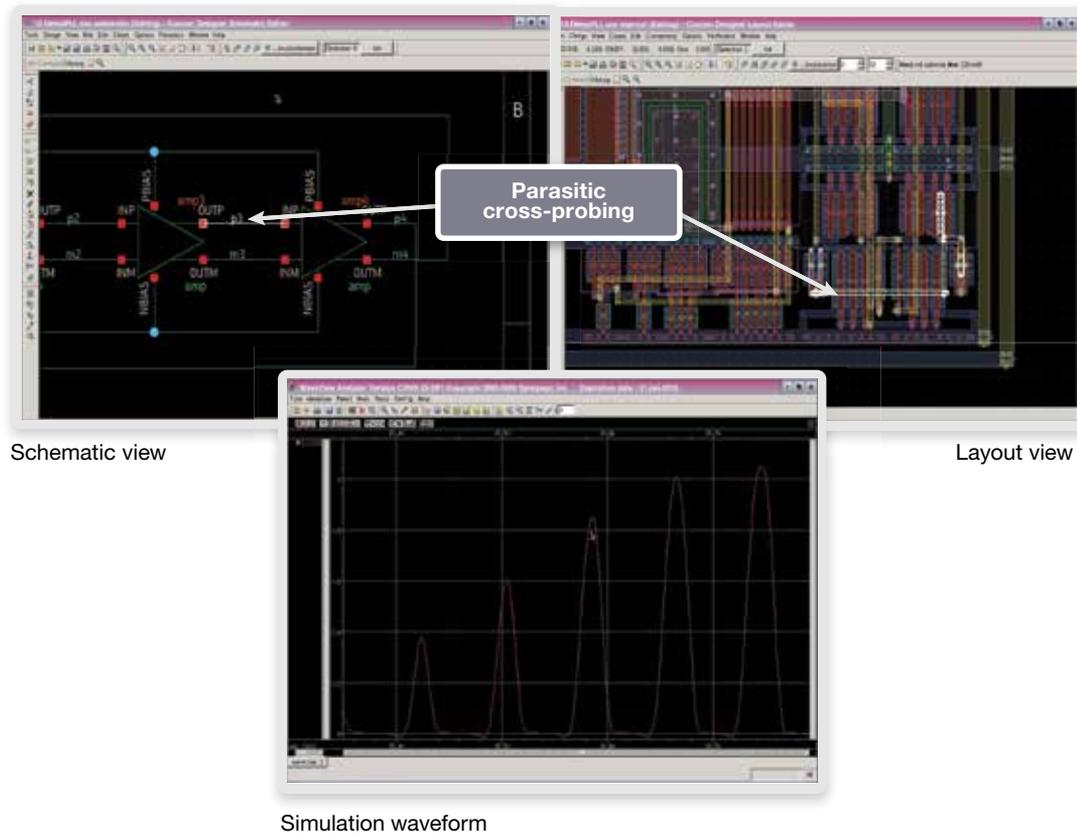**Parasitic cross-probing**

Layout view

Simulation waveform

Figure 6: StarRC integration with custom design environments, such as Galaxy Custom Designer, enables productive cross-probing and simulation debugging

- Selective device parasitic handling
- Flexible parasitic reduction
- Automated power net extraction optimization (TARGET_PWRA)
- Transparent simulation setup
- License queuing
- User-control reduction of parasitic netlists
- Advanced reduction features for simulation productivity

Specifications

File Format Support

StarRC supports the following industry-standard formats and interfaces:

- Layout data in: GDSII, LEF/DEF, Milkyway, NDM, IC Compiler, IC Compiler II, IC Validator, Hercules™, Mentor Graphics® Calibre®
- Output formats: GPD, SPEF, DSPF, SPICE

Platform/OS

- IBM® RS/6000® AIX® (64)
- x86 Red Hat® Enterprise Linux® (64)
- x86 SUSE® Linux (64)

For more information about this product, sales, support services or training, contact your local Synopsys sales representative or call 1.650.584.5000.

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