SpyGlass DFT ADV

RTL Testability Analysis and Improvement

Overview

SpyGlass® DFT ADV performs RTL testability analysis and improvement, enabling designers to fine-tune their RTL early in the design cycle to predictably meet their manufacturing and in-system test coverage goals. The tool's extensive design-for-test (DFT) rule checking and RTL fault coverage estimation capabilities help designers pinpoint testability issues early in the flow (Figure 1) and thus avoid test bottlenecks downstream that can lead to time-consuming design iterations.

Key Benefits

- Shortens test implementation time and cost by ensuring RTL or netlist is scan-compliant
- Improves test quality by diagnosing DFT issues early at RTL or netlist

Key Features

- Lint checking and analysis for DFT
- RTL stuck-at and transition fault coverage estimation
- Intuitive, integrated debug environment with cross-probing among views

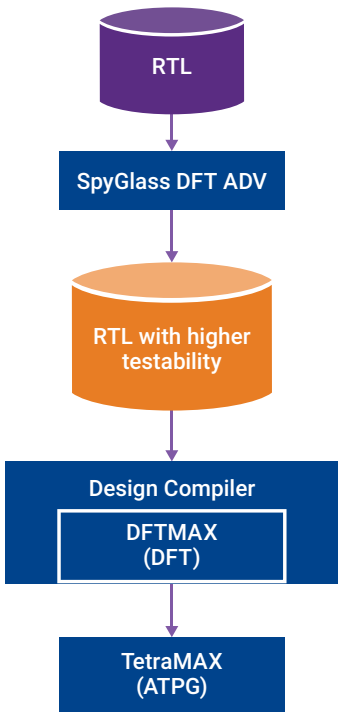

Figure 1: SpyGlass DFT ADV addresses testability issues early in the design flow.

Lint Checking and Analysis for DFT

SpyGlass DFT ADV performs lint checking to ensure the RTL or netlist can achieve maximum ATPG coverage. The tool verifies the design meets scan DRC requirements, providing detailed audit reports that help designers identify missing test constraints and make appropriate modifications to the design to address scan issues. It also verifies that a multi-voltage design complies with low-power DFT rules. For example, one type of check ensures that low-power constraints are compatible with scan test requirements; another type, applicable to netlists, verifies that scan chains do not cross voltage domains without level shifters.

Checking for Test Robustness

Testability profiling assesses test robustness – the susceptibility of test patterns to electrical glitches – and identifies RTL constructs that limit maximum stuck-at and transition fault coverage. Rule violations always reference the RTL so that designers know exactly where to make changes. To easily diagnose testability issues in the RTL, SpyGlass DFT ADV provides an intuitive, integrated debug environment that enables cross-probing among views (Figure 2).

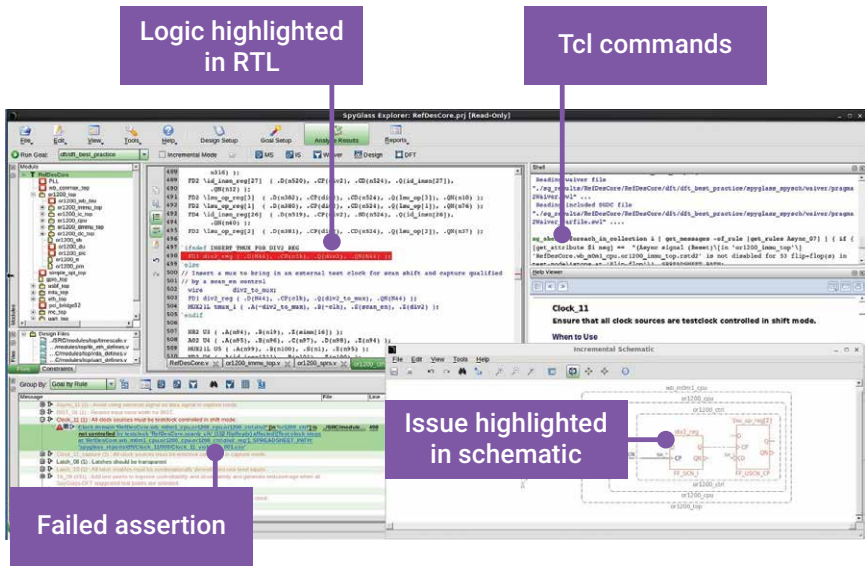

Figure 2: Integrated debug environment enables cross-probing among views to easily diagnose testability issues.

Random Pattern Analysis

A fault is deemed hard-to-detect if it has a very low probability of detection in a test composed entirely of randomly generated patterns. SpyGlass DFT ADV analyzes random pattern coverage to identify hard-to-detect faults, and suggests changes at the RTL to meet testability goals. The random pattern coverage estimation is displayed in the hierarchal fault browser in SpyGlass DFT ADV. Designers can quickly zoom into the blocks that have significant low coverage and further analyze which portion of the design leads to poor coverage.

Uncovering At-Speed Test Issues

Resolving at-speed test issues at the RTL can save weeks of effort. SpyGlass DFT ADV identifies timing closure issues caused by at-speed tests, which often achieve lower fault coverage than required even when full-scan is utilized and the stuck-at coverage is high. The following are examples of at-speed rules in SpyGlass DFT ADV that identify issues related to both timing closure and low coverage:

- PLL reference clock controllable from root level ports
- PLL control inputs controllable from root level ports
- All flip-flops controllable by PLL in at-speed test mode
- Asynchronous logic in the functional mode should not interact synchronously in test mode
- Synchronous logic in the functional mode should not interact asynchronously in test mode
- Required frequencies must be achievable

RTL Fault Coverage Estimation

SpyGlass DFT ADV provides estimates of stuck-at and transition delay fault coverage based on controllability and observability analysis. Coverage estimates are quick and patternless, thereby avoiding testbenches or long runtimes. Audit reports provide step-by-step guidance that allows designers to quickly and incrementally isolate the source of coverage loss.

Reference Methodology

The SpyGlass DFT ADV reference methodology provides a structured, easy-to-use, and comprehensive process for resolving RTL design issues, thereby ensuring high quality RTL with fewer design bugs. The methodology leads to fewer but more meaningful violations, thus saving time for the designer. The methodology documentation and rule sets are provided with SpyGlass DFT ADV.

Design Formats

SpyGlass DFT ADV supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Verification: VCD, FSDB