Synopsys RedHawk-SC

The gold-standard for power integrity and reliability signoff

Overview

Synopsys RedHawk-SC™ is the industry's trusted gold-standard solution for voltage drop and reliability signoff of digital designs, certified across all advanced foundry nodes. It delivers comprehensive, high-fidelity analytics to identify power integrity and reliability risks, enabling rapid resolution and first-time silicon success.

At the core of its innovation is SigmaAV™, a next-generation voltage analysis technology that provides high coverage and transforms traditional voltage drop analysis into a root-cause driven, application-aware solution. RedHawk-SC also incorporates advanced capabilities including reduced-order modeling for efficient full-chip and multi-die analysis, enabling faster turnaround and improved design convergence. Incremental what-if analysis and root cause analytics, tightly integrated with physical design, ECO and static timing analysis flows, enable early prevention of voltage drop issues, accelerate design closure, and maximize signoff productivity.

Built on Synopsys SeaScape™, the industry's first purpose-built big-data architecture for electronic system design and simulation, RedHawk-SC uniquely delivers the performance and capacity required for full-chip analysis of the world's largest semiconductor designs. It provides per-core scalability, flexible data access, instantaneous design bring-up, and scalable analytics—forming the foundation for next-generation AI-driven design workflows.

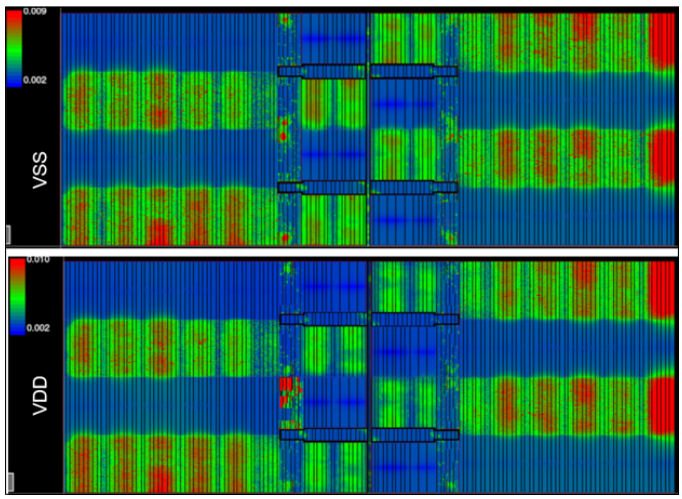


Figure 1: Voltage Drop Maps

Comprehensive Dynamic Analysis

RedHawk-SC provides the most comprehensive dynamic analysis coverage, enabling SoC and multi-die signoff with confidence using a wide variety of simulation approaches—RTL and gate vectors, smart vectorless analysis for functional and scan modes, mixed-mode simulation (vectorless and vector-based), and the unique SigmaDVD technology for high coverage.

Advanced Voltage Analysis, Noise Coverage with SigmaDVD

At advanced nodes (7nm and below), local aggressor switching dominates dynamic voltage drop behavior, making comprehensive coverage across activity scenarios increasingly challenging. RedHawk-SC addresses this with SigmaDVD, which identifies the precise local sources of power integrity issues across all instances early in the design cycle, delivering high local-noise coverage without the prohibitive runtime and compute cost of exhaustive transient simulations.

Building on this foundation, SigmaAV extends analysis beyond traditional IR drop detection by combining local, regional, and off-chip noise effects to uncover voltage drop scenarios often missed by conventional approaches. By decomposing voltage drop into its fundamental contributors, SigmaAV transforms power integrity signoff into optimization-driven workflows targeted for specific applications—whether for voltage drop prevention, timing closure, vector profiling, last-mile ECO, or system-level optimization. Path-aware SigmaAV further focuses voltage drop scenarios on timing-critical paths, enabling engineers to prioritize issues based on their true impact on performance and functionality.

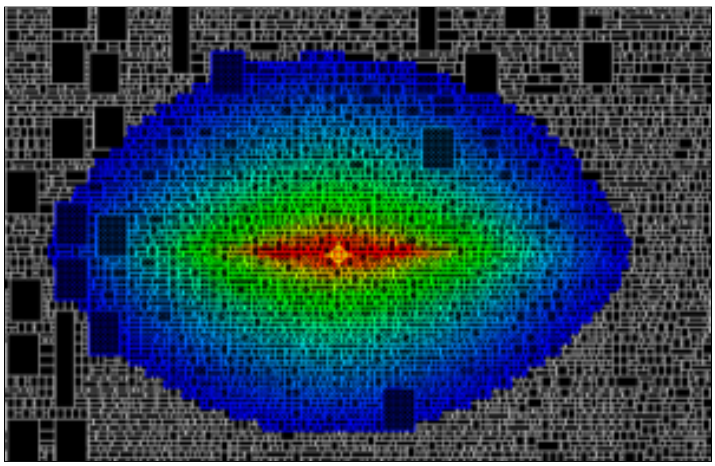


Figure 2: Neighboring cells color-coded by the level of voltage impact they have on the central victim cell

Root Cause Debug and DVD Diagnostics

RedHawk-SC provides a comprehensive debug environment to quickly debug and root-cause design weakness, voltage drop hotspots, and electromigration (EM) violations. An intuitive graphical user interface, integrated Explorer, and advanced diagnostics capabilities enable efficient input data validation and rapid issue isolation. Detailed aggressor-victim identification through DVD Diagnostics quantifies the impact of aggressors across both vector-based and vectorless scenarios, allowing designers to address root causes with minimum disruption to the design.

Fast Full-Chip Analysis with Hierarchical Modeling

As design sizes scale to billions of instances, early identification of power grid issues is critical. RedHawk-SC's Reduced Order Modeling (ROM) accelerates chip-level analysis, enabling rapid iteration and early identification of top-level power grid issues. ROM significantly reduces compute requirements while maintaining high accuracy for top-level analysis, providing an efficient method to identify grid construction issues and quantify the impact of packaging. It also provides context-dependent impact of chip-level design on blocks.

Electromigration and Reliability Signoff

Advanced nodes introduce increased complexity in electromigration (EM) due to higher current densities, smaller geometries, and increased thermal effects. RedHawk-SC addresses this complexity with comprehensive power and signal EM analysis. Thermal effects—driven by Joule heating, device coupling, and interconnect interactions—increase resistance, leakage, and stress, accelerating EM degradation and impacting reliability and device lifetime. By modeling both local and global thermal interactions, RedHawk-SC enables accurate thermal-aware EM analysis and statistical EM budgeting across the full design. Its signoff-certified power and signal EM engines ensure reliable validation for the most advanced foundry nodes.

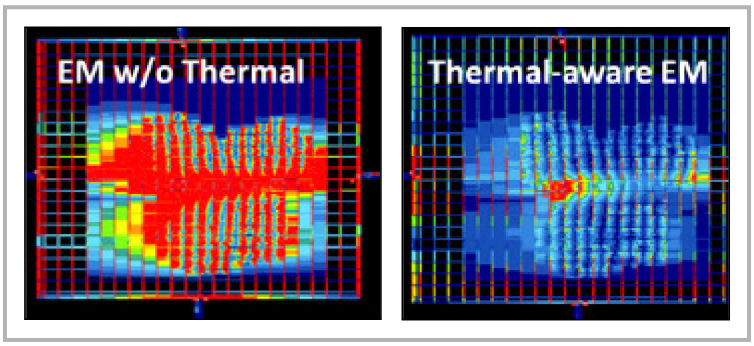


Figure 3: Thermal-aware EM analysis

Multiphysics-Aware Design, ECO, and Timing Signoff

At advanced nodes, traditional margin-based design methodologies lead to overdesign, larger die sizes, and longer schedules. RedHawk-SC integrations with Synopsys Fusion Compiler, PrimeClosure, and PrimeTime enable early voltage drop avoidance, accelerate design closure, and improve PPA.

Unlike conventional vector-based and vectorless approaches that provide limited coverage in identifying voltage drop hotspots, RedHawk-SC's SigmaDVD and SigmaAV technologies provide comprehensive coverage of voltage drop noise scenarios. This unique coverage enables robust IR-aware early design decisions, last-mile ECOs, and robust timing signoff. RedHawk-SC's root-cause analytics identify precise fixes in power grid, cell placement, and cell sizing. Further, its what-if analysis capability improves ECO productivity by evaluating voltage drop for only the affected regions, avoiding full-chip transient re-simulations.

Built on RedHawk-SC's coverage, analytics, and what-if capabilities, Fusion Compiler, PrimeClosure, and PrimeTime integrated solutions incorporate voltage drop as an optimization metric during physical design, deliver an automated timing-driven voltage drop ECO flow that achieves high fix rates with minimal design impact, and reduce margin pessimism and minimize timing escapes through voltage-aware timing signoff.

Multi-Die EMIR Analysis

RedHawk-SC's multi-die EMIR analysis delivers a flexible, end-to-end solution for power and signal integrity verification across advanced packaging designs. It supports the full design lifecycle—from early-stage power-delivery network (PDN) quality checks and bump placement validation to detailed signoff analysis capturing inter-die coupling and shared power network effects. High-fidelity power integrity analysis is enabled by a specialized extractor optimized for non-Manhattan geometries and a Full-Resolution IR Model (FIRM) with per-bump granularity enables hierarchical analysis. RedHawk-SC integrates seamlessly with the Synopsys 3DIC Compiler exploration-to-signoff platform, enabling multi-die and advanced packaging co-design and optimization within a single design environment.

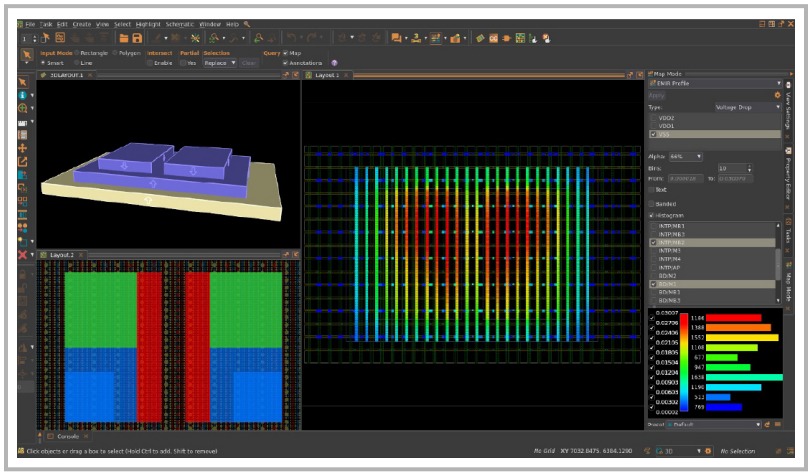


Figure 4: Multi-view voltage drop heatmap viewed in 3DIC Compiler

Chip-Package-System Analysis

RedHawk-SC enables co-optimization of chip and package power delivery network. Using Chip Power Models (CPMs) and Chip Thermal Models (CTMs), it models on-die electrical and thermal behavior and integrates these with package and system PDNs. This enables scalable system-level electrothermal simulation, allowing designers to optimize chip, package, and system power delivery with greater confidence and reduced overdesign.

AI-Driven Analysis—Built for the Agentic Era

RedHawk-SC supports next-generation AI-driven, agentic design workflows that require rapid exploration and iterative optimization. Built on a scalable, cloud-native platform, it reduces the cost of analysis and enables fast evaluation of multiple design scenarios without repeated full-chip processing. This capability enables intelligent, AI-assisted power integrity analysis, accelerating decision-making and expanding design exploration beyond traditional power integrity signoff.

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