SYNOPSYS®
Silicon to Software™

PrimeTime

Golden Timing Signoff Solution and Environment

Overview

Signoff users have a few key requirements for their signoff tool of choice: runtime and capacity to handle their largest chip size requirements, efficient multi-scenario analysis to verify timing across all corners and modes, margin control to reduce over-design and maximize chip performance, and accuracy to ensure correlation to silicon.

The Synopsys PrimeTime® Suite addresses these requirements by delivering fast, memory-efficient scalar and multicore computing, and distributed multi-scenario analysis and ECO fixing, while using variation-aware Composite Current Source (CCS) modeling that extends static timing analysis (STA) to include crosstalk timing, noise, power and constraint analysis.

PrimeTime Suite

The Synopsys PrimeTime suite, including PrimeTime, PrimeTime SI, PrimeTime ADV, and PrimeTime PX, provides a single, golden, trusted signoff solution with smarter approaches to timing, signal integrity, power, timing constraint and variation-aware analysis. It delivers HSPICE® accurate signoff analysis which helps pinpoint problems prior to tapeout, thereby reducing schedule risk, ensuring design integrity, and lowering the cost of design.

This industry gold-standard solution improves your team's productivity by delivering fast turnaround on development schedules for large and small designs while ensuring first-pass silicon success through greater predictability and the highest accuracy.

Benefits

HSPICE-Accurate Results Minimize Over-Design

HSPICE-accurate analysis pinpoints timing problems quickly and reduces ECO fixing time. Use of CCS models provides consistent results for static timing, signal integrity, power, and variation-aware analysis. Path-based analysis is available to zero-in on your most challenging timing paths. On-chip variation modeling and variation-aware analysis deliver additional margin control. This helps designers avoid the over- and under-design of chips, reducing costs and saving time from design schedules.

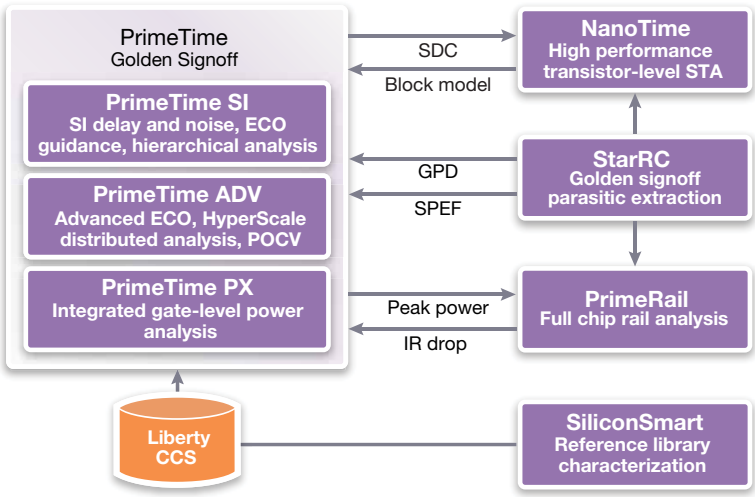

Figure 1. Galaxy Signoff Solutions

Integrated Design Environment Improves Productivity

The unified analysis environment in the PrimeTime Suite enables designers to perform complete timing, signal integrity, timing constraint, power and variation-aware analysis in a single environment. This improves designer productivity, reduces set-up steps, and minimizes the number of interface files created and used. It also leads to faster time-to-results because identical operations, such as timing and slew calculations, are not repeated. Costs are minimized by eliminating the need for multiple point tools with associated support costs.

Fast Turn-Around Time

PrimeTime offers a range of solutions to reduce the time required for analysis and signoff. Highly scalable multicore support reduces the time required for static timing and signal integrity analysis by taking advantage of the runtime benefits of threaded parallel processing. Distributed Multi-Scenario Analysis (DMSA) allows multiple scenarios to be run concurrently, which reduces wall clock time and produces a single comprehensive timing report.

High Capacity

PrimeTime performance and capacity improve release over release to take full advantage of the latest multicore compute hardware available in server farms. PrimeTime uses disk-caching for scalable multi-threading delivering fast performance in a low memory footprint.

Comprehensive Signoff

Comprehensive timing and design rule checking, extensive design constraint annotation and delay reporting allow ASIC and COT designers to signoff with confidence knowing that all aspects of their designs have been analyzed.

Advanced Node Support

PrimeTime supports the latest process node requirements at 7-nm and below, including advanced waveform propagation technology that accurately models waveform distortion at advanced nodes, especially in ultra-low voltage FinFET technology.

PrimeTime

The Synopsys PrimeTime static timing analysis solution is the most trusted and advanced timing signoff solution for gate-level designs. It is the standard for gate-level static timing analysis with the capacity and performance for 750+ million instance chips being designed at 10-nm and below. PrimeTime static timing analysis and StarRC™ parasitic extraction are key components of the Galaxy™ Design Platform.

The PrimeTime STA solution provides designers with extensive timing analysis checks, on-chip variation analysis techniques, golden delay calculation, advanced modeling, unmatched productivity and ease-of-use, a graphical user interface and industry-wide ASIC vendor signoff and foundry support.

The PrimeTime static timing analysis solution provides the foundation and environment for a suite of extensions in signoff analysis. In addition to timing analysis, PrimeTime SI, PrimeTime ADV and PrimeTime PX deliver extensions for signal integrity analysis, advanced ECO guidance and variation-aware analysis, and leakage and dynamic power analysis.

Golden Delay Calculator

PrimeTime's built-in RC delay calculator uses parasitic information and CCS libraries to calculate cell and interconnect delays with SPICE-like accuracy. The delay calculation and parasitic annotation reporting capabilities enable designers to debug and pinpoint timing problems. The PrimeTime delay calculator supports voltage and temperature scaling between libraries. This enables multi-voltage analysis without the need to maintain a large collection of libraries for each unique Process Voltage Temperature (PVT) point.

Advanced On-Chip Variation (AOCV) Analysis

At 65-nm and above, the traditional approach of using a global derate margin to account for on-chip variations (OCV) can provide margin control to account for process variation. At process nodes below 65-nm, PrimeTime's AOCV modeling capability extends OCV analysis to deliver an improved method of adding margin in a design. AOCV uses context-specific derate factors that consider location and logic depth of each path being analyzed, providing a more accurate method of assigning on-chip variation margins.

Advanced Latch Analysis

PrimeTime provides analysis of the latch-based designs used in power-sensitive applications. Both PrimeTime timing analysis and ECO guidance take the timing characteristics of latches into account. Support for advanced latch analysis allows ECO fixes to be appropriately distributed up- and downstream from latches.

Distributed Multi-Scenario Analysis (DMSA)

Signoff verification requires analysis of many individual scenarios that represent different operational modes and PVT corners. Analyzing and managing the analysis of these scenarios is simplified with PrimeTime's Distributed Multi-Scenario Analysis (DMSA) capability. DMSA allows designers to run distributed timing analysis simultaneously across multiple scenarios, thereby reducing overall turnaround time. Accompanying visualization capabilities accelerate the debug of multi-scenario analysis results.

Additional Features in PrimeTime

- Extracted Timing Models (ETM)
- UPF (Unified Power Format) support
- Graphical User Interface (GUI) enabling timing analysis and visualization using schematics, histograms, tables, and tree graphs
- Session save and restore
- ASIC vendor signoff and foundry support
- Extensive support for industry-standard input and output file formats

PrimeTime SI

With shrinking process geometries and rising clock frequencies for nanometer designs, signal integrity (SI) effects such as crosstalk delay and noise (or glitch) propagation can cause functional failures or failed timing. The PrimeTime SI solution extends the PrimeTime static timing analysis and signoff environment by adding accurate crosstalk delay, noise (glitch), and voltage (IR) drop delay analysis to address signal integrity effects at 90-nm and below.

Easy Deployment and Use

PrimeTime SI is easy to use and adopt. It utilizes the familiar PrimeTime flow and environment, with common commands, user interface, reports and attributes.

Comprehensive SI Analysis

The unified approach of signal integrity and timing analysis delivers a comprehensive and efficient method to analyze noise and crosstalk delay effects on timing. Analysis in a single tool enables faster results while improving designer productivity.

Accurate Crosstalk Delay, Noise (Glitch) and IR Drop Analysis

Signal integrity effects are interdependent and need to be analyzed in the context of timing. PrimeTime SI uses an integrated delay calculation engine with the PrimeTime STA engine to accurately model and compute timing deviations due to crosstalk and IR drop (See figure 2). PrimeTime SI has the capacity and performance to perform accurate noise calculation, detection, and propagation on the largest designs today.

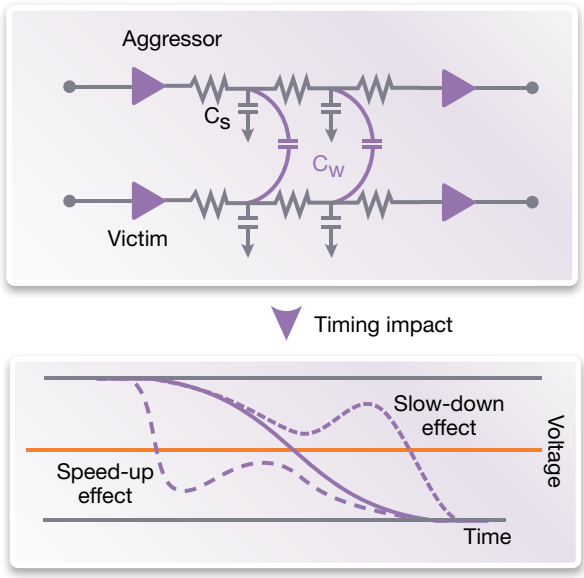

Figure 2. Crosstalk Delay Analysis Pinpoints Crosstalk Timing Failures

Simultaneous Multi-Voltage Aware Analysis

Multi-voltage designs require exhaustive analysis of cross voltage domain paths to ensure all worst-case paths are identified under all voltage combinations. Simultaneous multi-voltage aware analysis (SMVA) completes analysis of all cross-domain paths under all voltage scenarios in a single run, without the need for margining that can add pessimism.

HyperScale

With HyperScale, PrimeTime allows users to easily migrate from flat design analysis to hierarchical block-level analysis and full-chip distributed timing analysis, using mainstream compute resources available in private computing clouds. The hierarchical methodology supports both top-down and bottom-up flows, with state-of-the-art, timing-accurate context generation. This enables HyperScale block-level model analysis to be re-used throughout the flow, instead of re-analyzing the same blocks over and over at each level. The 5X – 10X performance and memory improvements reduce both compute resource cost and schedule risk, for current and future designs.

Constraint Analysis

PrimeTime improves designer productivity through look-ahead timing constraint analysis and debug technology tuned for the Synopsys Galaxy Design Platform. Early feedback on constraint quality leads to more efficient runtimes and better quality of results in synthesis, physical implementation and static timing analysis tools.

PrimeTime SI provides an intuitive interactive environment for designers to assess the correctness and consistency of timing constraints. This helps to eliminate trial-and-error iterations during implementation and results in more predictable schedules.

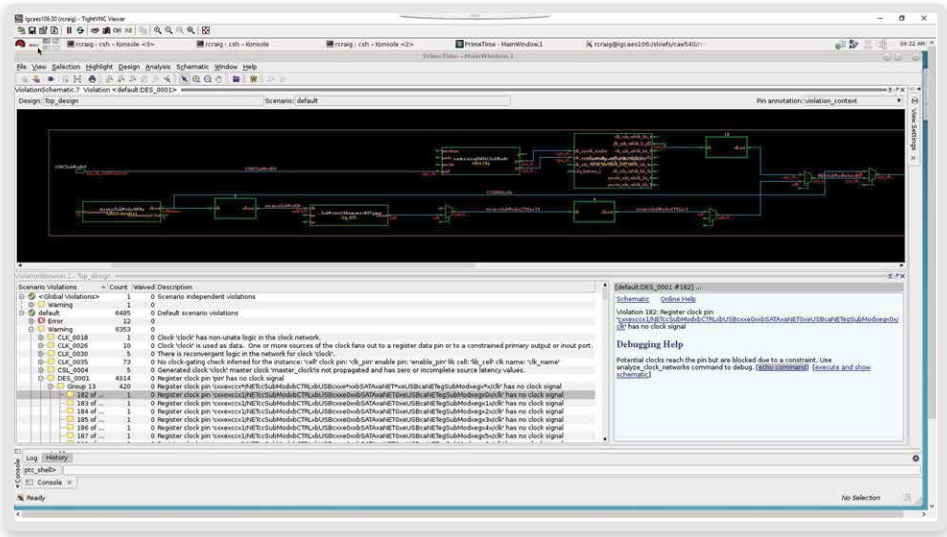

Figure 3. PrimeTime Constraint Analysis Interactive Environment

Mode Merging

With increased design complexity available at smaller process nodes, comes the need for additional operating and test modes. This can increase the number of scenarios required for timing closure and signoff. PrimeTime SI mode merging technology identifies superset modes that together replicate how a given design is constrained by the original individual mode constraints.

Mode merging uses the PrimeTime distributed multi-scenario analysis (DMSA) infrastructure, and can be added to an existing PrimeTime setup for a multi-scenario design.

Additional Features in PrimeTime SI

- Reduces false violations by considering slew propagation, timing windows, and logical correlation of signals
- Advanced waveform propagation accounts for waveform distortions at 20-nm and below that can impact timing
- SPICE deck output

PrimeTime ADV

PrimeTime ADV offers advanced technology to extend the scope of signoff-driven ECO closure, and provide a next-generation on-chip variation solution.

Physically-Aware Multi-Scenario ECO Guidance

PrimeTime's signoff-accurate ECO guidance enables a fast ECO closure flow. Optimal fixes for both timing and DRC violations are identified using the composite view available in the PrimeTime multi-scenario timing environment, avoiding iterative bottleneck analysis associated with multi-scenario ECOs. PrimeTime's integrated ECO solution offers timing-aware DRC fixing for maximum capacitance, transition and fanout, and timing fixes that honor DRC.

ECO guidance is resource efficient, working either on a single box or a distributed compute farm. In the event that limited hardware resources are available, ECO can be completed where the number of scenarios is less than the number of available hosts.

Physically-aware ECO Guidance works closely with IC Compiler's Minimum Physical Impact (MPI) technology, allowing routing and placement-aware timing, noise and DRC violation fixes that accelerate timing convergence by minimizing disruption to an existing layout — something that's especially important for congested designs.

In a hierarchical implementation and signoff flow, PrimeTime provides ECO guidance that complies with physical hierarchy specifications, including multiply-instantiated modules (MIMs) and multi-voltage configurations.

ECO Power Recovery

PrimeTime ECO Guidance can take advantage of positive timing slack to identify power reduction changes to the netlist without creating new timing violations.

PrimeTime ECO power recovery reduces total power and frees up available space for later ECO opportunities. After timing is closed, a final leakage recovery step gains additional power reduction with zero impact to physical design.

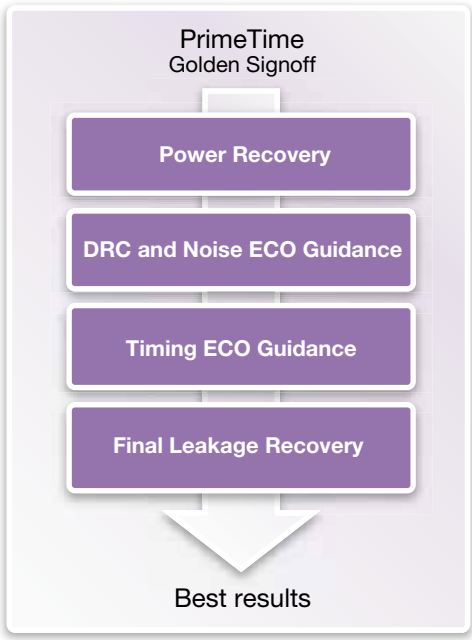

Figure 4. PrimeTime ECO Power Recovery Flow

Parametric On-Chip Variation (POCV) Analysis

POCV is the next generation of variation analysis targeted at 14/16nm processes and below. It provides a lightweight statistical margining approach to variation margining. It offers Graph and Path-Based Analysis pessimism reduction, along with improved ECO turnaround time.

Additional Features in PrimeTime ADV

- Automatically distributed HyperScale STA

PrimeTime PX

The PrimeTime PX solution expands the PrimeTime timing and signal integrity environment to deliver dynamic and leakage power analysis. Designers have a single, unified analysis environment for timing, signal integrity and power analysis that is anchored by the PrimeTime static timing solution.

By combining timing, signal integrity and power analysis into a single tool environment, common operations (e.g. netlist and parasitic reading) are not repeated. The PrimeTime PX solution delivers up to 2X faster time-to-results (TTR) over separate, standalone solutions. As an integral part of the PrimeTime environment, power analysis can be performed using PrimeTime commands, reports, attributes and debugging features.

Full-Chip Timing, SI and Power Analysis

The unified analysis environment allows designers to perform leakage and dynamic power analysis along with timing and SI analysis. Designers can understand the trade-offs and effects of leakage and dynamic power in the context of complete timing, signal integrity and power analysis by adopting the easy-to-use PrimeTime PX methodology.

Vector-Free Dynamic Power Analysis

Vector-free dynamic power analysis allows power analysis to be performed without waiting for switching data from simulation. By using the PrimeTime tool's accurate timing windows, vector-free analysis enables power analysis early in the design flow to identify blocks with the highest power consumption, sooner.

Additional Features in PrimeTime PX

- Event-based dynamic power analysis using VCD or SAIF
- RTL and gate-level VCD and SAIF support
- Instantaneous and cycle-accurate peak power analysis
- Average power analysis
- State-dependent leakage power analysis
- Analysis of advanced low power design techniques: multi-voltage, coarse-grain MTCMOS
- Clock tree power estimation
- Power analysis driver GUI window
- Distributed Peak Power Analysis
- UPF support
- Supports industry-standard NLDM and CCS Power libraries

Galaxy Signoff Modeling and Platform Support

Advanced Modeling

The PrimeTime Suite provides a wide range of advanced modeling support. Extracted Timing Models (ETM) are provided, in .lib format, for cell-based reusable IP and physical design flows. A complete set of validation, debugging and model merging features are also provided.

HyperScale hierarchical analysis technology offers hierarchical analysis and signoff, with the information captured in saved sessions acting as block models.

OS Platform Support

The following platforms are supported: Linux RHEL 6.6+, Linux SUSE 11+. See the Synopsys Release Specific Support documents for further details.

About Galaxy Design Platform

The Galaxy Design Platform is an open, integrated design platform with tools and IP, enabling advanced semiconductor design. Anchored by Synopsys' industry-leading semiconductor design tools, the Galaxy Design Platform incorporates consistent timing, SI analysis, common libraries, delay calculation, constraints, testability and physical verification to provide a convergent flow from RTL, all the way to silicon. The Galaxy Design Platform helps reduce design time, decrease integration costs and minimize the risks inherent in advanced, complex semiconductor design.

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