PrimeRail

In-Design Rail Analysis for Place-and-Route Engineers

Overview

PrimeRail is the rail analysis technology foundation for IC Compiler In-Design Rail Analysis™. Invoked directly from IC Compiler, In-Design Rail Analysis utilizes embedded PrimeRail analysis and fixing guidance technology to enable designers to easily perform power network verification throughout physical implementation. By identifying and fixing voltage-drop and electromigration issues earlier in the flow, designers can eliminate costly iterations late in the design process. Built on industry gold standard PrimeTime® SI and StarRC™ signoff technologies, PrimeRail offers high-accuracy, full-chip SoC static and dynamic rail analysis to accelerate design closure.

IC Compiler In-Design Rail Analysis

Working in concert with IC Compiler's Power Network Synthesis (PNS) and In-Design Physical Verification™ capabilities, In-Design Rail Analysis provides designers with the most comprehensive power network design and verification solution.

Traditional approaches to power network design consist of separate implementation and verification steps, often performed by different engineers using many tools and environments in a complex flow. With leading-edge SoC designs, this approach often results in multiple iterations between physical implementation and signoff, adding significant risk to project schedules. By eliminating complicated data exchanges and with no new tools to learn, IC Compiler users can now ensure the integrity of their power network early and frequently during the physical implementation process, avoiding late-stage surprises close to tapeout. In-Design Rail Analysis works in tandem with IC Compiler's Power PNS capability to enable designers to efficiently implement, optimize and refine power networks, significantly reducing overdesign. In addition, In-Design Physical Verification helps ensure that power networks are design-rule clean as refinements and fixes are implemented. IC Compiler's ecosystem of PNS, In-Design Rail Analysis and In-Design Physical Verification today offers the fastest and most comprehensive solution for power network design.

Full-chip SoC Static and Dynamic Rail Analysis Solution

PrimeRail technology offers designers flexibility with both static and dynamic rail analysis for full-chip SoC designs. Dynamic analysis is a fine-grain, time-based rail analysis of all resistive, capacitive and inductive components of the design whereas static is a coarser average analysis for resistive components only. With much faster runtime, static rail analysis can be use more frequently throughout the physical implementation process. This enables designers to quickly find and fix violations such as inadequate or missing via connections, unconnected power regions, or undersize power rails as design changes are made. Dynamic rail analysis can be used to fine-tune the power network, for example, to isolate local noise by adding enough decoupling capacitors without causing too much leakage.

Comprehensive rail analysis of today's SoCs requires the accurate and efficient modeling of memories, custom IP and analog blocks. PrimeRail's unique and flexible Dynamic White-box Modeling (DWM) capability is designed to deliver compact, high-accuracy macro models based on transistor-level parasitics and circuit simulation. DWM models are easy to create using CustomSim™ and StarRC. In addition, the simulation-free DWM Lite modeling capability allows for over 10X faster creation of macro models for use earlier in the flow where it's not critical to have the highest accuracy.

Advanced Low Power Design Support

Leakage power has become a daunting challenge in sub-90-nm designs, especially for mobile, consumer and wireless applications. Advanced low power design techniques, such as multiple supply voltages, dynamic voltage scaling and MTCMOS power-gating switches, are frequently used to reduce leakage power consumption. However, the increasing use of these switches and power on/off operations increases current gradients, exacerbating power network integrity problems due to high inrush current.

PrimeRail performs full-chip dynamic voltage-drop and EM analysis of low power multi-voltage designs using MTCMOS power gating switches. It offers accurate modeling of power switches, analysis of inrush current and wake-up time during power-up to active mode. PrimeRail's multi-mode analysis enables designers to optimize the power-on sequence of the MTCMOS switches to mitigate the risks of design failure. In addition, the "what if" analysis capability allows easy design trade-offs to meet both leakage and voltage-drop requirements throughout the design implementation process.

Key Features

▸ Integrated IC Compiler In-Design Rail Analysis environment
  • Pushbutton setup and data integrity checking to streamline flow
  • Milkyway™ database integration to eliminate costly tool input and outputs
  • Integrated display environment overlaying maps directly with layout
  • Integrated error browser with detailed reporting and fixing guidance to rapidly pin-point, isolate and fix potential issues
  • Ability to run, analyze, fix and debug throughout the IC Compiler flow from design planning, pre-layout and post-layout to chip finishing

▸ Integrated with Galaxy™ Implementation Platform
  • Built on PrimeTime SI and StarRC signoff technologies
  • Built-in library characterization utility for Liberty™ Composite Current Source (CCS) power library support

▸ Comprehensive dynamic and static rail analysis
  • Voltage drop analysis
  • Electromigration analysis
  • Power network weakness analysis
  • Inrush current analysis for power switches
  • Decoupling capacitance analysis
  • Vector-free and vector-based dynamic analysis
  • Multi-mode analysis of advanced low power designs using multiple voltage islands and MTCMOS/power-gating cells
  • Frequency domain core model generation with S parameters in SPICE
  • Electromagnetic interference (EMI) analysis
  • "What-if" analysis for debugging and optimization

▸ Full-chip SoC capabilities
  • Up to 3 million instances-per-hour performance
  • Dynamic modeling of memories and mixed signal blocks
  • Embedded hierarchical power network parasitic extraction
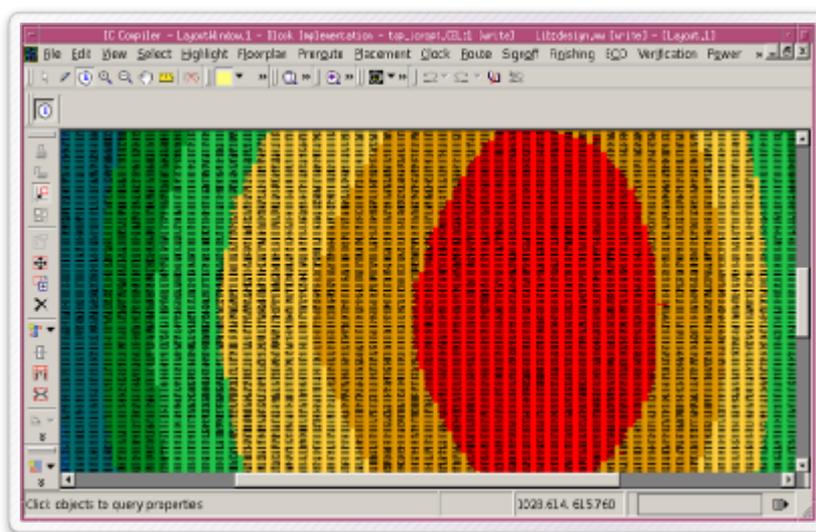 • System and package RLC support
  • Accuracy within 10% of HSPICE®

Figure 1: IR Drop Map Displayed Directly in IC Compiler

Specifications

System requirements

▸ DRAM: 512MB, recommend 1GB

▸ Swap Space: 512MB, recommend 2GB

▸ Installation disk space: 250MB baseline plus 250MB per platform

▸ Design disk space depends on the circuit size, recommended minimum 500MB

Platform support

▸ AMD64

▸ AI32

▸ Sun32 and Sun64

▸ SUSE32

▸ SUSE64

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