

PrimePower

Delivers accurate dynamic and leakage power analysis

Overview

The Synopsys PrimePower tool is a power analysis solution that accurately analyzes full-chip power dissipation of cell-based designs throughout the design implementation process, from early estimation to signoff.

PrimePower provides accurate power analysis reports for SoC designers to make timely design optimizations to achieve power targets; the supported power types include peak power, average power, clock network power, leakage power, and multi-voltage power.

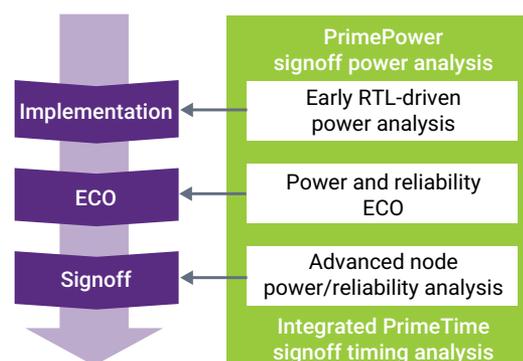
By closely integrating with the PrimeTime tool, the golden industry standard for timing and signal integrity signoff, PrimePower expands PrimeTime® timing and signal integrity analysis solution to deliver accurate dynamic and leakage power analysis.

PrimePower Capabilities

The PrimePower tool provides vector-free and vector-based peak power and average power analysis. The vectors to PrimePower are either RTL- or gate-level simulation results in the Value Change Dump (VCD) format, Fast Signal Database (FSDB) format, or Switching Activity Interchange Format (SAIF).

PrimePower builds a detailed power profile of the design based on the circuit connectivity, the switching activity, the net capacitance, and the cell-level power behavior data in the Synopsys database format(.db) library. PrimePower also supports Nonlinear Power Model (NLPM) libraries. It calculates the power behavior for a circuit at the cell level and reports the power consumption at the chip, block, and cell levels.

When power analysis is complete, you can view design data and analysis results in the Graphical User Interface (GUI), including power maps and waveforms, for visual power debugging.



Features:

Full-Chip Timing, SI and Power Analysis

The unified analysis environment allows designers to perform leakage and dynamic power analysis along with timing and SI analysis. Designers can understand the trade-offs and effects of leakage and dynamic power in the context of complete timing, signal integrity and power analysis by adopting the easy-to-use PrimeTime PX methodology.

Vector-Free Dynamic Power Analysis

Vector-free dynamic power analysis allows power analysis to be performed without waiting for switching data from simulation. By using the PrimeTime tool's accurate timing windows, vector-free analysis enables power analysis early in the design flow to identify blocks with the highest power consumption, sooner.

Averaged Power Analysis

For purely averaged power analysis, PrimePower supports propagation of switching activity based on the default settings, user-defined switching data, or switching data derived from an HDL simulation (either RTL or gate-level).

Time-based Power Analysis

For extremely accurate power analysis with respect to time, the tool supports analysis based on the RTL or gate-level simulation activity over time.

The tool uses an event-driven algorithm to calculate the power consumption for each event. For time-based power analysis, the tool generates detailed average and peak power waveforms, as well as power reports.

Multi-voltage Power Analysis

PrimePower supports power calculation for cells with multiple power supplies either using UPF, non-UPF, power domains, or power rails to specify power intents. Scaling the power consumption per power net by the specified voltage is also supported.

Clock Network Power Analysis

PrimePower supports activity propagation through the clock network to calculate power consumption of the clock network in the averaged power mode.

PST-based Power Analysis

A Power State Table (PST) is a UPF construct which defines the legal combinations of voltage values and states of the power and ground supplies for all supply sets in the design. PrimePower supports UPF PST-based power analysis in the average mode

Cycle-accurate Peak-power Analysis

PrimePower uses the RTL switching activity data to calculate power in the cycle-accurate peak power analysis mode. In this mode, the tool calculates the power per event accurately, and generates power waveforms at the clock-cycle resolution. Use the results to determine the cycle during which maximum power consumption occurs in a design.

Cell Electromigration Analysis

PrimePower supports cell electromigration analysis to identify cells whose toggle rates exceed the maximum toggle rate based on the current types (either average, rms or peak) listed in the electromigration table. This allows you to identify and resolve possible electromigration issues early in the flow.

The cell electromigration analysis is supported in both averaged and time-based power analysis modes.

Concurrent Event Analysis

The tool provides concurrent event analysis that enables multi-process distributed processing to help reduce memory resources or excessive runtime when analyzing a full-chip design with multiple gate-level FSDB files.

This feature is supported only in the time-based power analysis.

Distributed Peak Power Analysis

PrimePower supports distributed peak power analysis using the distributed multi-scenario analysis (DMSA) infrastructure and PrimeTime distributed timing analysis to help reduce memory resources or excessive runtime when analyzing a large chip design.

Concurrent Multi-rail Analysis

PrimePower supports the multi-rail analysis to check the contribution of each rail in a single run for time-saving purposes.

Close Integration with the PrimeTime Suite

You can invoke PrimePower for power calculation within the PrimeTime tool. The integration of timing, signal integrity, and power eliminates the redundant set-up and calculation steps required when using separate standalone tools.

Link with the RedHawk™ Analysis Fusion in IC Compiler™ II

The RedHawk power integrity solution is integrated with the IC Compiler II implementation flow through the RedHawk Analysis Fusion interface. PrimePower supports the generation of the power consumption and static timing data (STA) to perform voltage drop analysis on the power and ground network.

Power ECO Analysis

PrimePower generates reports on peak power, clock power, and cell electromigration reliability for creating change lists.

Additional Features in PrimeTime PX

- Event-based dynamic power analysis using FSDB, VCD or SAIF
- RTL and gate-level FSDB, VCD and SAIF support
- Instantaneous and cycle-accurate peak power analysis
- State-dependent leakage power analysis
- Analysis of advanced low power design techniques: multi-voltage, coarse-grain MTCMOS
- Clock tree power estimation
- Power analysis driver GUI window
- UPF support