SYNOPSYS®
Predictable Success

NanoTime

Transistor-level Static Timing Analysis Solution for Custom Designs

Overview

With process geometries reaching 90-nanometers (nm) and below, there are many nanometer effects that can impact timing. Accurate analysis of these effects is required to identify real timing issues.

Synopsys' NanoTime tool is the next-generation transistor-level static timing analysis solution that addresses the emerging challenges in signal integrity (SI) analysis associated with custom designs.

NanoTime offers concurrent timing and SI analysis, accuracy within five percent of HSPICE®, and the performance required to analyze complex transistor circuits overnight. Its seamless integration with Synopsys' PrimeTime® product enables full-chip analysis of designs that includes both gate- and transistor-level blocks. NanoTime is a key component of the Synopsys custom design verification solution that includes CustomSim® and HSPICE for circuit simulation and ESP-CV for symbolic simulation.

The Challenge

Accurate transistor-level analysis of crosstalk-delay

As designs go down to 90-nm and below, crosstalk-delay becomes more than 25% of total delay. Prior solutions including traditional static timing analysis with optional 3rd party crosstalk delay analysis do not provide the accuracy and productivity that is required. Concurrent timing and SI is a must to achieve silicon success.

Full chip timing verification

Transistor- and gate-level static timing analysis need to work together to achieve full chip timing verification (i.e) a seamless and accurate timing analysis flow from custom design to gate-level with PrimeTime is required. To achieve higher productivity, NanoTime has the same commands as PrimeTime whenever they are applicable.

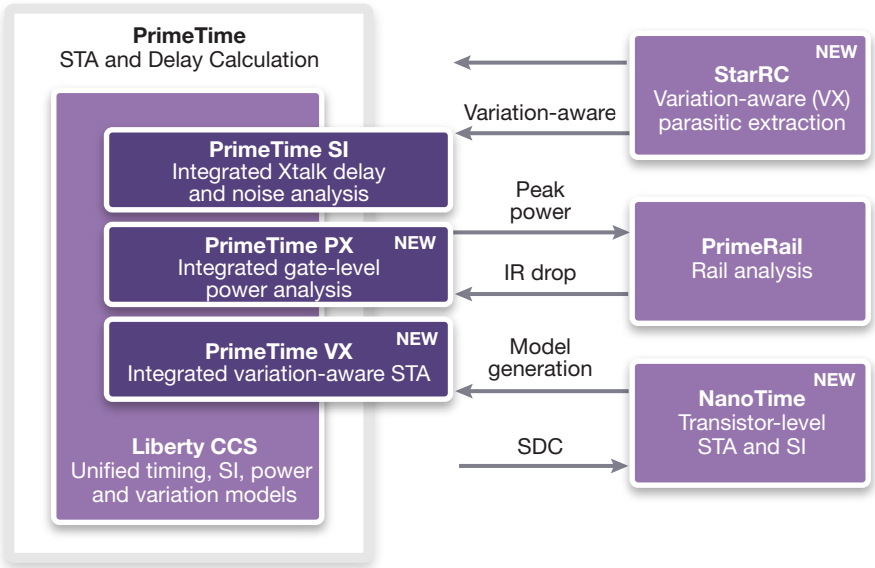

Figure 1. Galaxy Signoff Solutions

The Solution

NanoTime offers higher predictability and improved productivity to custom designers over prior solutions. Its concurrent timing and SI features enable designers to accurately and quickly identify timing issues early and avoid expensive silicon re-spins. NanoTime helps ensure silicon-accurate analysis and delivers overnight analysis results for complex million-transistor designs. NanoTime further boosts designers' productivity by offering significant ease-of-use features, including interactive static timing analysis, extracted timing model (ETM) creation, and seamless integration with PrimeTime.

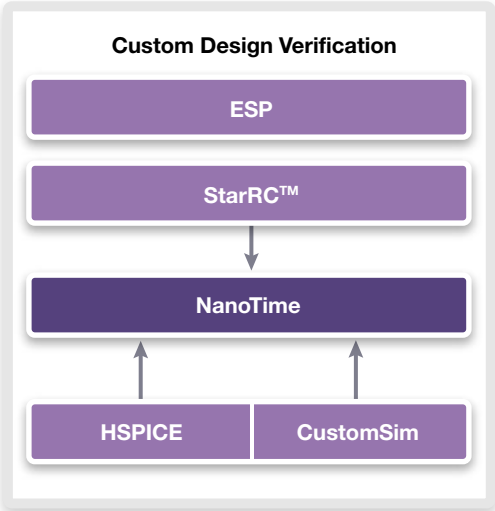

Figure 2. Custom Design Verification Solution

Key Features and Benefits

- Concurrent timing and signal-integrity (SI) analysis provides higher predictability and better productivity over existing solutions. NanoTime offers integrated timing and crosstalk-delay analysis to achieve higher silicon accuracy.
- With its unmatched ability to recognize complex custom design structures, embedded NanoSim technology for dynamic circuit evaluation and the state-of-the-art RC reduction algorithm, NanoTime delivers accuracy within 5% of HSPICE
- Ease of use features improves productivity. The ease-of-use features include easy setup with Tcl, the Synopsys common command interpreter; interactive timing analysis that allows multiple analyses in a single session and a seamless flow with PrimeTime that supports Synopsys Design Constraints (SDC).
- New algorithms that result in a five-fold increase in performance over existing solution without sacrificing accuracy

Additional Features

- Provide longest and shortest path reports, considering crosstalk impact
- Set up, hold and transparency timing checks for sequential circuits
- Timing checks for complex circuit designs (domino logic, pass gates, gated clocks)
- Slack analysis
- Intelligent false path suppression
- Post-layout analysis with RC back-annotation
- Direct advanced model support
- On-demand dynamic simulation capability for complex data and clock structures
- Multiple voltage support
- Transparent Extracted Timing Model generation that natively works with PrimeTime
- Ability to merge timing models
- Industry-standard support, Liberty™, SDC, SPF, SPEF

For more information about this product, please contact your local Synopsys representative or call 1-800-388-9125.

SYNOPSYS®
Predictable Success
Synopsys, Inc. • 700 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

03/10.CE.18-18438.