SYNOPSYS®
Accelerating Innovation

# Laker Flat Panel Display

## Overview

*The Laker™ Flat Panel Display (FPD) solution is the leading technology in flat panel display design and layout. With built-in functions custom-tailored for flat panel layout, Laker FPD enables FPD designers to create, edit and verify the flat panel design from reticle plan and circuit design to panel layout in a single high-performance environment.*

## Major Benefits

- Reduce total design cycle time by reticle and panel co-design
- Reticle cost optimization based on automatic mask and shot planning
- Schematic-driven flow with reference FPD device PDK
- Correct-by-construction panel layout creation
- High quality of results from specialized FPD routing automation
- Tight integration with signoff physical verification

## Major Features

### *Reticle and Panel Co-Design*

- Comprehensive flow covers pre-layout mask and shot planning along with panel outline, post-layout exposure simulation, analysis and job file generation.
- The panel outline size is estimated and verified along with rapid panel prototype by AA-IC-FPC place-and-route automation

### *Schematic-Driven Flow*

The schematic-driven layout (SDL) flow in Laker FPD helps create an optimized layout that is DRC/LVS-correct in less time — without sacrificing layout area. Both netlist and schematic views are included with the Laker layout editor for an intuitive SDL working environment, which includes:

- Schematic view and design browser
- Advanced layout editor, including rule-driven layout, flight-line guidance and short detection
- Realize, place, route, and edit a physical layout that is DRC- and LVS-correct

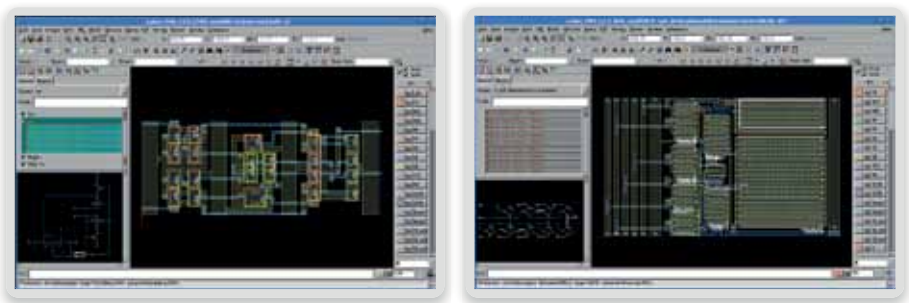

**Figure 1: Laker FPD schematic-driven flow with reference device PDK**

### *Unique Routing Automation*

- Advanced Equal Resistance Route (AERR), Gateway Model Realizer (GMR) and Ladder Route make fan-in and fan-out connections quickly and accurately following user-defined patterns and parameters
- In-route integration of metal slit, cut corner enables one-pass routing with predictable resistance control

### *Parasitic Extraction*

- Resistance measurement reports routing path resistance of automated and manual routes for immediate feedback of resistance values

### *Physical Verification*

- Built-in rule-driven DRC, LVL and ERC features support interactive editing
- Tight integration with signoff physical verification tools such as IC Validator to browse and fix design rule and LVS violations

**For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.**

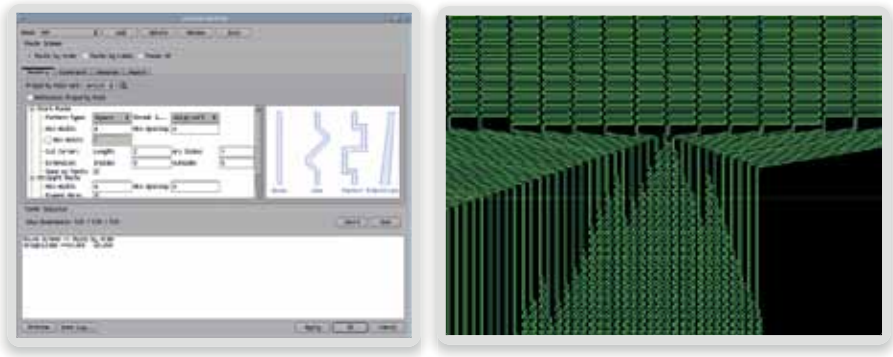

**Figure 2: Advanced Equal Resistance Route with width adjustment and cut corner**

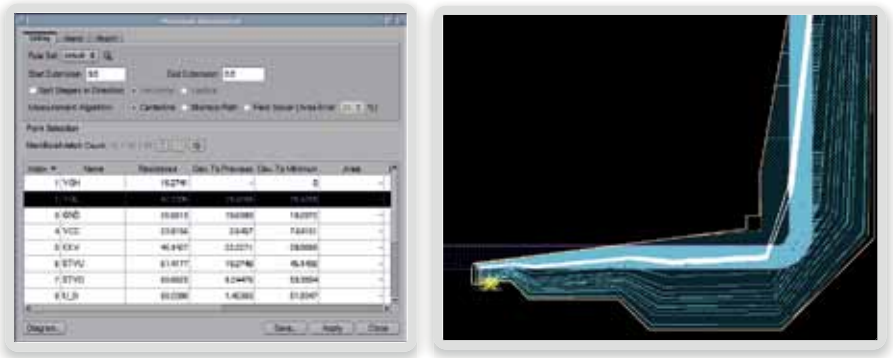

**Figure 3: Resistance report of Gateway Model Realizer with metal slit**