

IC Validator

**High-performance
DRC/LVS physical
verification
substantially reduces
time-to-results**

Overview

Synopsys® IC Validator™ is a comprehensive physical verification signoff solution that delivers performance scalability and broad runset support for all mainstream and advanced process nodes. The Design Rule Checking (DRC) and Layout Versus Schematic (LVS) physical verification engine substantially reduces the time to results through near-linear scalability across hundreds of CPU cores. IC Validator delivers DRC signoff within hours on some of the industry's largest designs with 10 billion+ transistors and die sizes greater than 800mm².

IC Validator is seamlessly integrated with IC Compiler® II place and route system for In-Design physical verification. This award-winning technology accelerates design closure for manufacturing by enabling independent signoff-quality analysis and automatic repair within the implementation environment.

Benefits

- Industry leading performance enabled by distributed processing scalability to hundreds of CPU cores
- Signoff certified by all major foundries with broadest qualification and runset availability
- In-Design physical verification in IC Compiler II for enhanced productivity
- Innovative Automatic DRC Repair (ADR) for rapid discovery and repair of DRC errors
- Timing-aware fill to ensure manufacturability and high yield while meeting timing targets
- LVS-aware Shortfinder to quickly and easily identify multiple shorts in a single run
- Integration with StarRC™ parasitic extraction, Custom Compiler™ full-custom solution, and other third party layout tools for increased designer productivity



High Performance and Scalability

The complexity of physical verification has grown substantially at the advanced process nodes. To address the capacity and performance requirements of physical verification at advanced nodes, IC Validator is architected for scalability and efficient utilization of available hardware.

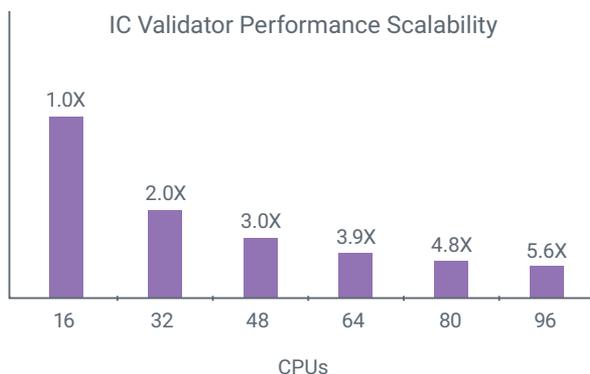


Figure 1: IC Validator near-linear performance scalability

Features

- Multi-threading significantly shortens execution time on modern multicore CPUs
- Near linear scalability across a distributed computing network with hundreds of CPU cores enables completion of most physical verification tasks overnight (Figure 1)
- On-Demand load balancing provides intelligent job scheduling, keeping all cores equally busy to minimize the time required to complete a job
- Memory-aware scheduling distributes jobs to avoid the delays caused by paging when memory is exceeded

Comprehensive Physical Signoff Solution

Synopsys' IC Validator is the proven high performance and comprehensive signoff physical verification solution (Figure 2). Trusted by leading semiconductor companies and used in hundreds of production designs, IC Validator offers a physical verification tool suite including DRC, LVS, Programmable Electrical Rule Checks (PERC), dummy fill, and Design For Manufacturing (DFM) capabilities.

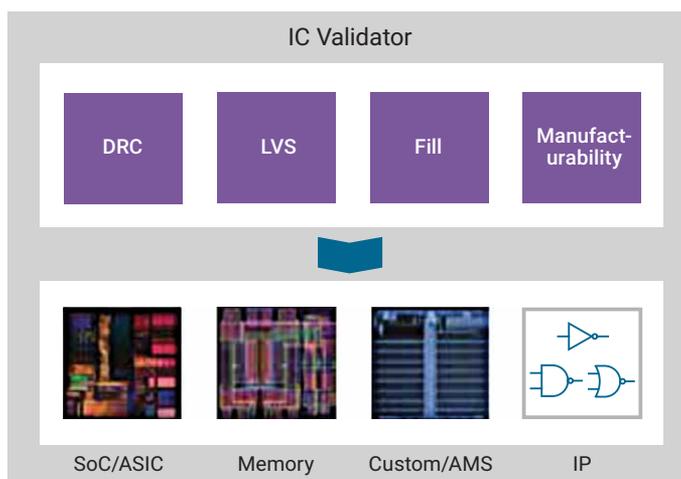


Figure 2: IC Validator comprehensive physical signoff solution

Foundry Qualification

Comprehensive foundry qualification is a necessary component of any successful physical verification solution. IC Validator is signoff certified by all major foundries. IC Validator is actively in production use for FinFETs, SOI and traditional technologies at established process nodes and advanced emerging process nodes by leading foundries.

Layout-vs-Schematic (LVS)

The most important aspect of an LVS solution is the power and efficiency of its debug environment. IC Validator VUE and Shortfinder tools quickly identify errors, such as text-level shorts, for rapid repair and revalidation. VUE is a graphical environment to display and cross-probe between layout and schematics, together with a sophisticated error management system. IC Validator LVS device extraction supports leading edge technologies where device parameters are often affected by their proximity to neighboring devices through layout dependent effects (LDE).

Fill-to-Target Technology

IC Validator's Fill-to-Target technology is a tile-based parametric fill engine that inserts the right shapes in the right places to give superior planarity and smooth fill density, even around macros. This correct-by-construction approach improves yield and speeds turnaround time by replacing the traditional iterative fill-analyze flow with a single-pass flow.

Double, Triple, Quad Patterning

Manufacturing at 20nm and below usually relies on Double Patterning Technology (DPT), which requires that a design be decomposable into two overlapping layout patterns. IC Validator offers comprehensive support for double patterning. IC Validator includes a native coloring (decomposition) engine based on flexible coding of DPT rules, and supports advanced capabilities such as stitching rules. With In-Design technology, IC Validator provides signoff quality decomposition checking and automatic repair of DPT conflicts. (Figure 3).

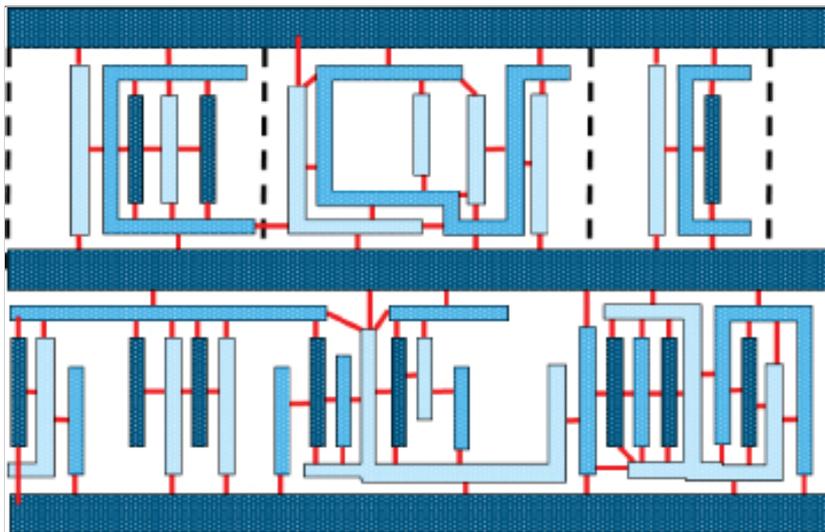


Figure 3: Signoff quality double, triple and quad patterning verification

Pattern Matching

IC Validator's pattern matching efficiently expands IC Validator's rule-based signoff engine for pattern-driven verification. This capability makes it possible to quickly identify and automatically correct manufacturability hotspots in a design by comparing against a library of known problematic layout patterns. IC Validator's patented pattern matching technology eliminates the need for convoluted rules, and with almost zero runtime penalty per pattern, it significantly reduces the time to achieve manufacturing compliance.

Error Visualization

To maintain efficient physical verification, rapid visualization and error correction are as important as fast physical verification runtime. IC Validator includes the IC Validator VUE visualization tool, which provides an easy-to-use, intelligent error navigation and prioritization system for efficient review and correction of DRC and LVS issues, double, triple and quad patterning conflicts, and manufacturing-limiting patterns. Using IC Validator VUE, layout engineers can quickly and easily scan physical verification errors in the IC Compiler II environment, as well as other widely used layout editors.

Integration with StarRC

IC Validator LVS has an efficient working flow with Synopsys StarRC for parasitic extraction. IC Validator supports end-to-end hierarchical parasitic extraction that minimizes physical flattening and simplifies extraction by implementing a single pass flow, providing a major performance increase over the double extraction flow of previous generation tools.

Integration with Custom Compiler

IC Validator works together with Synopsys' full-custom solution, Custom Compiler, to support a tightly integrated DRC and LVS-enabled custom design flow. Both IC Validator and Custom Compiler fully support the OpenAccess database. In addition, Custom Compiler is integrated with the VUE error navigator for rapid debug of DRC and LVS issues.

Enhanced Productivity with In-Design Physical Verification

IC Validator brings the power of full signoff physical verification constraints into the design phase with IC Compiler II, without imposing time-consuming stream-in and stream-out of layout data. Using In-Design physical verification, DRC and manufacturing issues are caught much earlier in the design cycle, reducing or eliminating late-stage surprises close to tapeout.

Automatic DRC Repair (ADR)

IC Validator's seamless integration with IC Compiler II enables an innovative layout auto-correction interface, which identifies DRC violations, including DPT decomposition violations and initiates automatic repairs. The corrections are applied by IC Compiler II to alleviate DRC and DPT errors, and then validated within IC Validator. In-Design integration makes it possible to maintain hotspot-free designs throughout implementation, further eliminating iterations with downstream analysis tools. ADR's tight find-and-repair loop enables rapid discovery and repair of errors, minimizing designer intervention and speeding time to tapeout. (Figure 4).

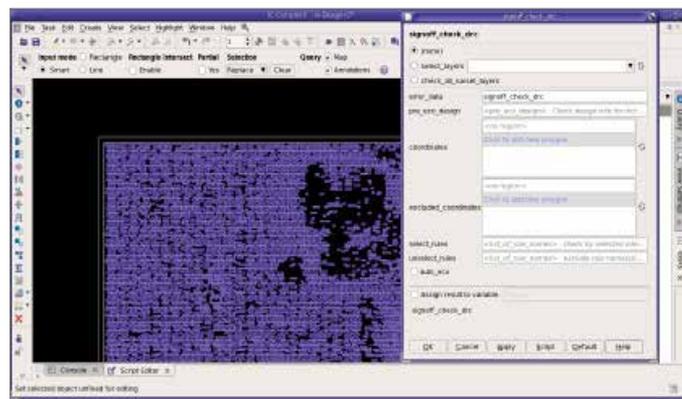


Figure 4: In-Design DRC in IC Compiler II

Incremental Layer-based, Rule-based and Area-based Verification

IC Validator and IC Compiler II integration enables intelligent incremental flows to eliminate unnecessary checking by restricting verification to the specific layer, rule or design area that needs validation. The tight integration provides a powerful tool dialog that allows the user to quickly select the rules, layers and region size for DRC checking, pattern matching, or adding metal fill. By automatically limiting the scope of the validation, more verification runs can be performed early in the design cycle, greatly reducing the number of full design verification runs, and shortening the time to results. (Figure 5).

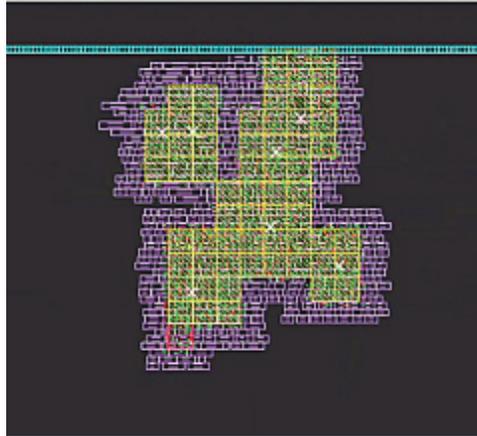


Figure 5: Area based incremental signoff DRC analysis

Timing-aware Fill

At advanced nodes, fill insertion is mandatory to ensure manufacturability and high yield. But excessive fill can lead to build-up of coupling capacitance, impacting timing and resulting in unpredictable iterations with design. In-Design technology with IC Validator enables single-pass fill implementation that is timing-aware to prevent such problems. Combined with IC Validator's fill-to-target technology, timing-aware fill efficiently balances timing and density and replaces multiple fill-analyze iterations with a single step. At the sub-20nm nodes, timing-awareness coupled with track-based fill enables higher fill densities along with greater control over fill density vs. timing impact.

Reliability Verification

In addition to being a comprehensive physical verification platform, IC Validator is also a reliability verification platform. PERC enables customized checking for EOS/ESD/ERC rules. IC Validator programmable PERC is a reliability solution that understands checking for issues that require only a netlist (Netlist Domain Checks or NDC), those that require a combination of both the netlist and layout shapes (Mixed-Mode Checks or MMC), and checks for current density and point-to-point resistance (CDC/P2P).

IC Validator programmable PERC leverages the power and wide-spread familiarity of the Python® scripting language for robust and easy rule creation. PERC elevates electrical rule checking from time-consuming and error-prone manual methods to high-speed automated reliability verification.