IC Compiler II

Industry Leading Place and Route System

Accelerating Time to Results on advanced Designs

Overview

IC Compiler™ II is the leading place and route system delivering industry-best quality-of-results (QoR) for designs across all process nodes, while enabling unprecedented productivity.

IC Compiler II is specifically designed to address today's aggressive performance, power area and time to market pressures with innovative solutions for flat and hierarchical design planning, early design exploration, placement and optimization, clock tree synthesis, routing, manufacturing compliance, and signoff closure challenges.

IC Compiler II is a complete netlist to GDSII system that includes early design exploration and prototyping, design planning, block implementation, and final chip assembly for handling advanced node designs. State-of-the-art technologies in IC Compiler II addresses complex design challenges and delivers industry-best QoR metrics, in terms of timing, power, area, signal integrity, design density, routability and manufacturability while providing the fastest design cycle times.

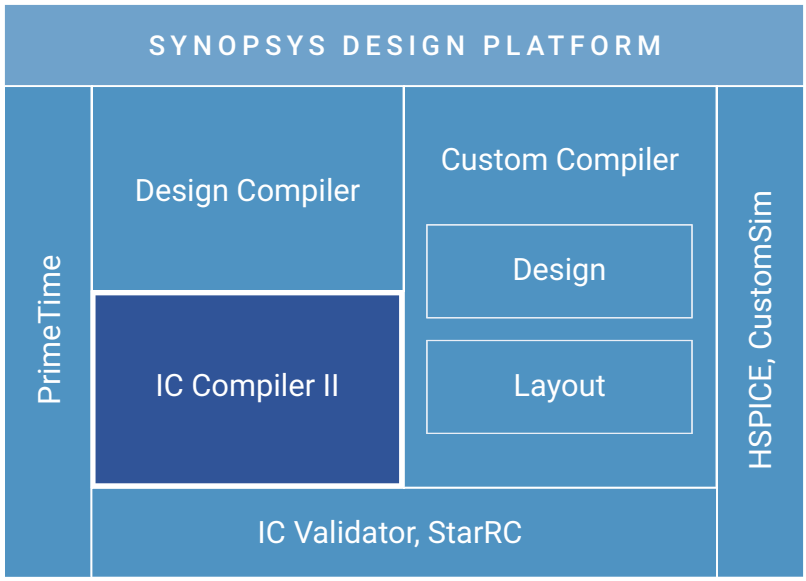

Figure 1: IC Compiler II Anchor in Synopsys Design Platform

IC Compiler II is centered on a new scalable architecture to handle the complex needs of advanced node designs. IC Compiler II has a natively hierarchical infrastructure to tackle designs in the order of hundreds of millions of instances. Built from ground-up to enable virtually any design style Out-Of-The-Box (OOTB), IC Compiler II's design planning produces the most optimal floorplan configurations in the shortest time. Multithreading and distributed processing of key engines enable fast design convergence and rapid Time To Results (TTR). An innovative, global, and analytical approach to optimization pushes the envelope on QoR, setting new standards for Performance Power Area (PPA).

IC Compiler II's award-winning Zroute digital router technology supports complex foundry FinFET, multi-patterning & EUV requirements across all process nodes to deliver a seamless flow from design planning to routing. A centerpiece in Synopsys Design Platform, IC compiler II is the only tool in the industry with tight correlation with PrimeTime®-SI, StarRC™ and IC Validator signoff engines.

Empowering Design Across Diversified Applications

The dizzying pace of innovation and highly diversified applications across the design spectrum are forcing a complete rethink of the place and route systems to design and implement differentiated designs in a highly competitive semiconductor market on schedule. Designers on emerging process nodes must meet aggressive PPA and productivity goals. It essentially means efficient and intelligent handling of 100s of millions of place-able instances, multiple levels of hierarchy, 1000s of hard macros, 100s of clocks, wide busses, and 10s of modes and corners power domains and complex design constraints and process technology mandates.

Delivering Fastest Design Performance

IC Compiler II offers a comprehensive set of technologies to meet the aggressive demands of ultra-high performance designs. IC Compiler II's new optimization framework enables physically-aware synthesis with congestion, layer assignment, and route-based optimization capabilities for best QoR. Additional technologies such as networking flow paradigm based clock tree synthesis and tight correlation to signoff engines delivers best design performance.

Powerful Chip-Level Cockpit

IC Compiler II's new data model enables designers to perform fast exploration and floorplanning with complex layout requirements. IC Compiler II can create bus structures, handle designs with n-levels of physical hierarchy, and support Multiply Instantiated Blocks (MIBs). A design data mismatch inferencing engine analyzes the quality of inputs and drives construct creation on the fly, delivering design insights even with "incomplete" data early in the design cycle. Concurrent traversal of logical and physical data models enables hierarchical Data-Flow Analysis (DFA) and fast interactive analysis through multi-level design hierarchies and MIBs. Data flow and feedthrough paths highlighted in Figure 2 allow analysis and manipulation through n-levels of hierarchy to complete early design exploration and prototyping.

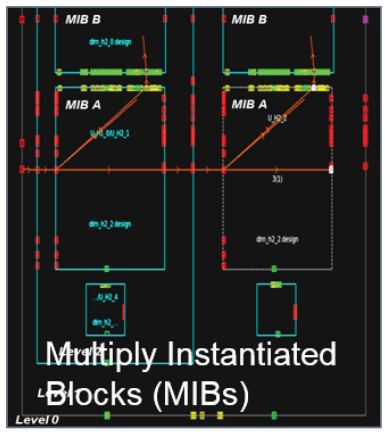

Figure 2: Fast interactive analysis through multiple-levels of physical hierarchy and MIBs

Pipeline-register-planning shown in Figure 3, provides guidance for optimal placement to meet the stringent timing requirements of high performance designs. Interactive route editor integrated which is advanced node aware shown in Figure 4, allows intricate editing and routing functions, including creation of special signal routes, buses, etc.

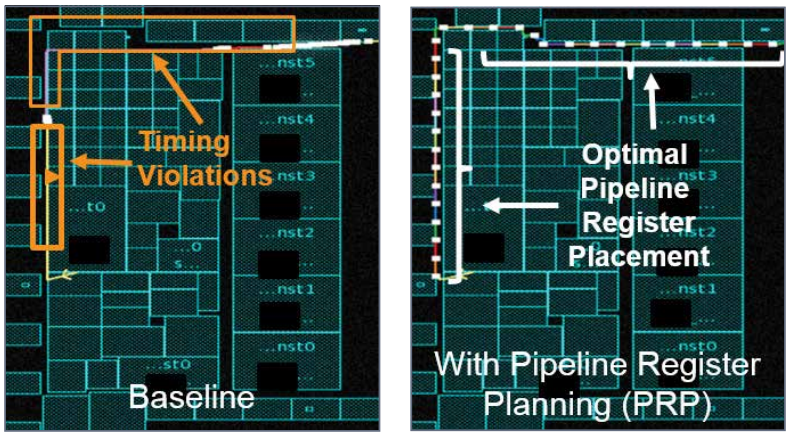

Figure 3: Pipeline register placement enables superior QoR for designs with complex buses

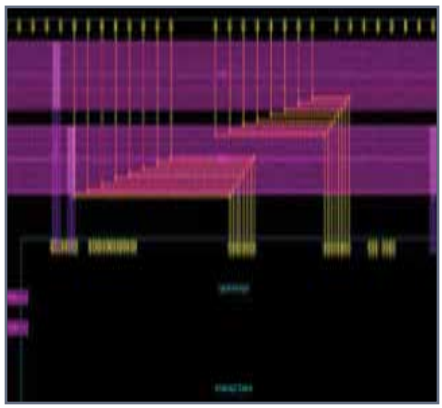

Figure 4: Comprehensive interactive layout editing critical for high speed designs

Global Optimization and Analysis

IC Compiler II features a new optimization framework built on global analytics. Shared timing and placement engines with synthesis engines enable physically-aware synthesis, layer assignment, and route-based optimization for improved QoR. MultiCorner MultiMode (MCMM) and MultiVoltage (MV) aware, level-based analytical algorithms continuously optimize using parallel heuristic algorithms. Multi-factor costing functions deliver faster results on both broad and targeted design goals. Logic remapping, rewiring and legalization interleaved with placement minimizes congested logic, resulting in simple localized logic cones. Advanced modeling of cell spacing automatically determines cell-spacing targets and minimizes design congestion. Advanced modeling of congestion across all layers highlighted in Figure 5 provides accurate feedback throughput the flow from design planning to post-route optimization. Emerging process nodes coupled with power sensitive applications make it extremely important to have early and accurate power and Electro Migration (EM) analysis. Power analysis shown in Figure 5 help make intelligent choices to manage power and mitigate IR.

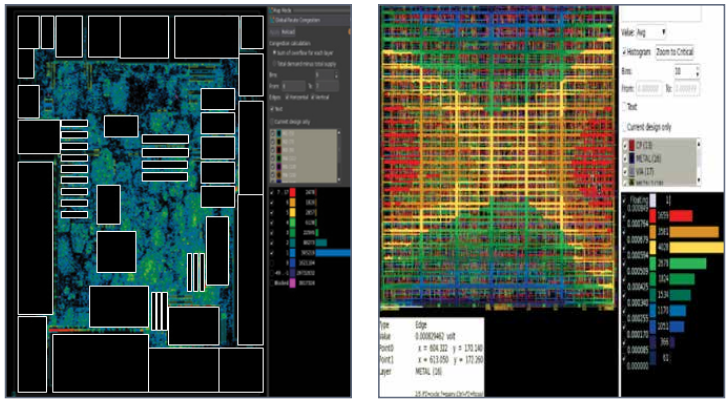

Figure 5: Intelligent and accurate analysis for congestion and power

High Performance and Robust Clocking Technology

IC Compiler II introduces new Clock Tree Synthesis (CTS) engines that follow a networking flow paradigm for better balancing of latency and skew. Sub-tree latency criticality is calculated up front and used to predict context-effects. CTS performs netlist traversal across all modes, optimally balancing routes per sub-tree while avoiding clock order dependencies. Robust distribution enables virtually any clock style, including mesh, multi-source, or H-tree topologies. Advanced analysis and debugging features perform accurate clock QoR analysis and debugging as highlighted in Figure 6.

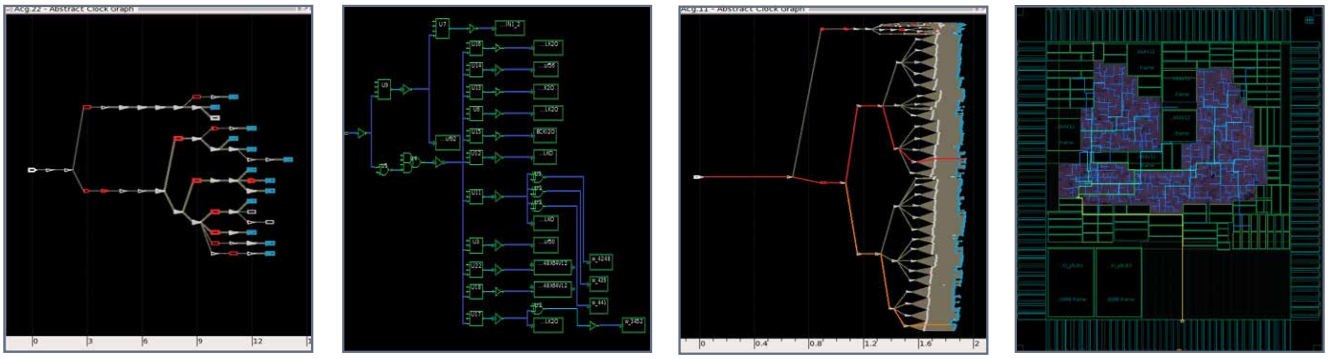

Figure 6: Accurate clock QoR analysis and debugging (a & b) Abstracted clock graph and schematic.
(c) Latency clock graph. (d) Colored clock tree in layout

Tight Convergence Implementation to Signoff

Addressing the growing metal stack variability in FinFET (FF) geometries, IC Compiler II leverages the industry-leading Zroute Global-Route (GR) technology to achieve best design convergence. GR-based layer assignment guides pre-route extraction and high-fanout-net buffer insertion follows routing topology for superior QoR. Final pre-route optimization uses high-accuracy timing models to perform final rebuffering and sizing and post-route optimization uses on-route re-buffering for minimal design disruption through to final design closure.

Lowest Power and Smallest Area

IC Compiler II introduces a comprehensive approach to managing power throughout the design process, delivering better energy-efficiency and smaller area for a variety of applications across all process nodes. IC Compiler II supports the Unified Power Format (UPF) for support advanced multi voltage design styles. Power optimization is performed throughout the design flow using concurrent optimization transforms to handle multiple cost metrics including power, timing, and area.

Total Power Optimization

IC Compiler II minimizes leakage with fast and efficient cell-by-cell power selection across HVT, SVT and LVT cells and varying channel lengths. This finer cell selection granularity allows intelligent power and performance based tradeoffs. Logic re-composition and cell-and-wire co-optimization, minimize wire length, and reduce dynamic power. Activity-driven power optimization uses VCD/SAIF, net toggle rates, or probability functions to drive placement decisions and minimize pin capacitances. Physically and Design For Test (DFT) aware multi-bit register banking optimizes clock tree structures, reduces area, and net length, while automatically managing clock, data, and scan chain connections.

Power-Focused Concurrent Clock and Data Optimization (CCD)

IC Compiler II expands the use of CCD optimization technology throughout the flow, targeted at boosting performance while significantly reducing power. Dynamic management of skew during placement makes it possible to significantly reduce clock area and clock network power. CCD balances sinks that are timing-critical, resulting in more efficient use of runtime and resources while ensuring no timing degradation. Available skew is used not only to meet datapath timing but also minimize its power consumption.

Tighter Signoff Correlation, Less Margin

To minimize design margin, IC Compiler II is MCMM-aware and employs a variety of novel technologies for faster design closure. A shared kernel with PrimeTime guides final optimization with golden signoff accuracy enabling the tool to extract the best QoR for designs. Advanced timing modeling capabilities including Parametric On-Chip-Variation (POCV) analysis, Signal-Integrity (SI) timing windows, advanced waveform propagation, and Path-Based-Analysis (PBA) further tighten implementation's drive better optimizations. Post-route physically-aware leakage recovery uses cell sizing and swapping with high accuracy costing to further minimize power.

Enhanced Designer Productivity

IC Compiler II brings technological breakthroughs to physical implementation that enable faster runtimes and larger capacity, opening opportunities to rethink the entire product development process. IC Compiler II achieves maximum throughput using extensive parallelization technologies, core engine speedups and flow enhancements.

Faster Completion for All Design Steps

IC Compiler II is architected from the ground up for speed and scalability. Its hierarchical data model consumes 2-3X less memory than conventional tools, boosting the limits of capacity to 500M placeable instances and beyond. Adaptive abstraction and on-the-fly data management minimize memory requirements and enable fast, responsive data manipulation. Near-linear multi-core threading of key infrastructural components and core algorithms such as database access and timing analysis, speed up optimization at all phases of design. Patented, lossless compact modeling and independent R and C extraction allow handling more Modes and Corners (MCMM scenarios) with minimal runtime impact.

Better Automation, Fewer Manuals Steps

Expansive use of automation in IC Compiler II boosts designer productivity and overall OOTB user experience. A natively-hierarchical multi-level design flow automatically shapes voltage areas and seamlessly handles pin constraints, groupings, and MIBs. Inter-voltage-area nets are buffered automatically with appropriate sizing of isolation buffers and level shifters. A fully-automated macro placer dramatically accelerates working with macro-dominated topologies. Automatic density control uses advanced modeling of cell spacing rules to determine spreading targets, minimizing manual tuning and accelerating runtime for downstream design steps. Fully integrated and advanced node compliant, shape and constraint driven custom router shown in Figure 7, allows optimal creation, editing, and managing special signals and busses. This is a key enabling technology critical for advanced designs with large and complex buses at the chip level.

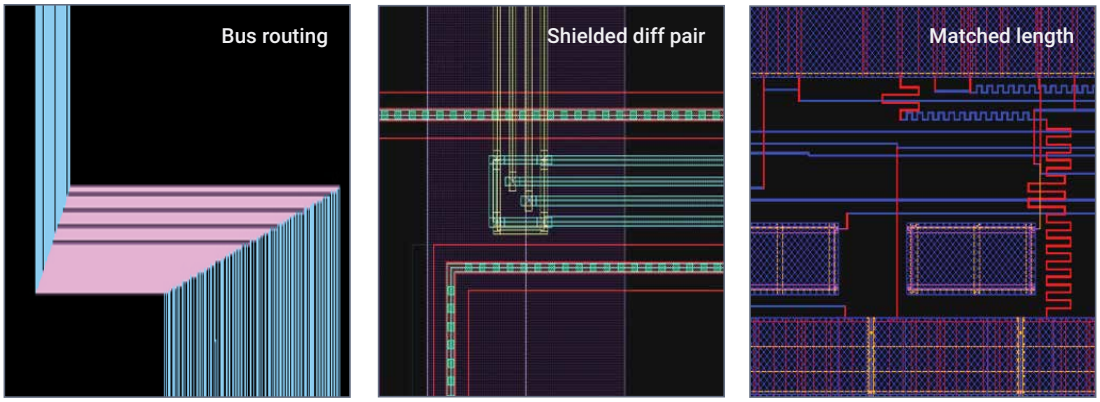

Figure 7: Fully integrated shape and constraint driven custom router

Synopsys Design Platform Links

As key part of the Synopsys Design Platform implementation system, IC Compiler II offers links to many industry-leading signoff tools through smart technology to accelerate design transition to signoff. In-design physical verification with IC Validator automates Design Rule Checking (DRC) violation repair from within implementation. In-Design flow also enables foundry and track based metal fill highlighted in Figure 8, to achieve high density and meet foundry signoff requirements.

Figure 8: IC Validator In-Design metal fill color aware metal fill, optimized for density and foundry requirements

Tight integration with Custom Compiler™ allows for high-accuracy custom routing with net-length and parasitic matching. In-design links to ANSYS enable Power-Ground (PG) integrity checking, static, and dynamic voltage drop analysis. A tightly linked, fully incremental Synopsys ECO flow with industry standard StarRC parasitic extraction and PrimeTime, automates and accelerates final timing closure while minimizing leakage power.

Industry's Richest Ecosystem

Modern silicon applications require the best performance and yield out of foundry processes. Close collaboration with foundry and ecosystem partners is key to ensuring maximum benefits across the entire range of available silicon technologies.

Better ROI at Emerging Nodes

IC Compiler II provide advanced node design enablement across major foundries and technology nodes—including 16/14nm, 12/10nm, 7/5nm, and sub 5nm geometries. Zroute digital router technology ensures early and full compliance with the latest design rules required for these advanced node technologies. Synopsys collaborates closely with all the leading foundries to ensure that IC Compiler II is the first to deliver support for early prototype design rules and support for the final production design rules. IC Compiler II design technologies maximize the benefits of new process technologies and offer optimal return on investment for cutting-edge silicon applications.

Optimal mW/MHz for Arm Cores

IC Compiler II features many innovative technologies that make it the ideal choice for high-performance, energy-efficient Arm® processor core implementation, resulting in industry-best milliwatts/megahertz (mW/MHz) for mobile and other applications across the board. Synopsys and Arm work closely together to offer optimized implementation of popular Arm cores for IC Compiler II, with reference flows available for Arm Cortex®-A high-performance processors and Mali GPUs. In addition, Arm offers off-the-shelf Artisan® standard cell and memory models that have been optimally tuned and tested for fast deployment in an IC Compiler II environment. Continuous technology innovation and close collaboration makes IC Compiler II the leading choice for Arm-based high-performance design.

Advanced Design at Established Nodes

IC Compiler II facilitates advanced design on advanced silicon technology nodes, enabling faster turnaround and more differentiated products. From meeting timing of high-speed interfaces to maximizing utilization of available die area, optimizing leakage power and automating multi-voltage feedthroughs, IC Compiler II is the ideal choice for advanced designs.