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GenSys

RTL Restructuring and Design Assembly

Overview

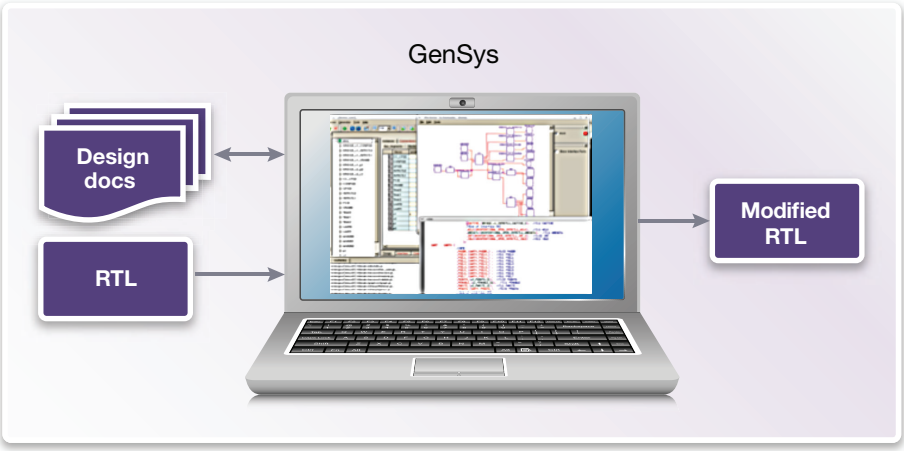
Increased IP reuse in SoC design creates challenges in managing source RTL for systems or subsystem assembly and in handling the RTL modifications needed when creating a new or derivative design. GenSys provides an environment to enable "correct-by-construction" RTL design assembly and includes management and modification tools for RTL restructuring that enables improved productivity for front-end designers.

Design Assembly

GenSys provides designers with an environment to perform architectural planning and optimization during chip or sub-design assembly processes. It supports bottom up and top-down methodologies for hierarchical design assembly, allowing users to change the hierarchy on the fly and create or edit components in place. GenSys also includes comprehensive connectivity checking and supports both interface and user-defined connection rules to drive fast completion of many connections. With an easy-to-use GUI, a Tcl command environment, spreadsheet interfaces and user customizable reports, GenSys facilitates clear communication of design specifications across team members.

RTL Restructuring

The process of capturing and managing RTL modifications on a large SoC design can be error-prone, often requiring complex and difficult-to-maintain user scripts. GenSys makes it easy to perform modifications such as hierarchy manipulation, swapping of IP or memory blocks, insertion of new RTL and restructuring of existing RTL. It includes schematic and hierarchy views with easy to use drag and drop capabilities, built-in analysis tools, RTL health checks, version tracking and mapping file output for use in formal verification. GenSys speeds up the task of design modification, ensures that no errors are introduced and enables efficient design reuse.



Key Benefits

- Enables “correct-by-construction” RTL assembly, reducing the time to create high-quality designs
- Provides an easy-to-use environment for RTL remapping and restructuring for new and derivative designs
- Enables effective design reuse and IP integration
- Helps dispersed design teams to create more consistent high-quality designs

Key Features

- Supports standard formats, including Verilog, VHDL, CSV (Microsoft Excel) and Tcl
- Provides batch and graphical use-models that are fully interchangeable
- Interface-based connectivity reduces user-defined connections
- User-definable auto-connect techniques help complete numerous connections
- Custom report generation through user defined templates

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