FPGA Design Solution for High-Reliability Applications

‣ Design Automation for High Reliability

‣ FPGA Technology Independence

‣ Best Quality of Results for High Performance

‣ Integrated SEU Mitigation Technologies

‣ Supports Industry Standards for DO-254, IEC 61508, and ISO 26262

‣ Signal Processing IP and Verification

‣ Industry Leading RTL Synthesis Technology

‣ Debug of an Operating FPGA, Directly from RTL Code

‣ Broad Language Support for Verilog, VHDL, VHDL-2008 and SystemVerilog

High-Reliability Implementation Solutions

FPGA designers creating applications that involve high radiation environments, human safety and that require high up-times, such as those in industrial, medical, automotive, communications, military, and aerospace segments, have special requirements for reliable design operation. These types of designs demand methodologies to implement designs that exhibit high levels of operational reliability without compromising performance. Applying its deep knowledge of FPGA design tools, Synopsys delivers high-quality, high-performance, and technology-independent solutions that address the demanding requirements of high-reliability applications. Synopsys' tools automate several proven methods for mitigating soft errors such as single-event upsets (SEUs) that are increasingly present in the latest FPGA process geometries. It used to be that radiation-induced soft errors were only a concern at high altitudes, and in mil/aero applications, but they have now become a concern for ground-level applications as well.

Synopsys' offers a high-reliability solution to help FPGA designers create products that are resistant to radiation-induced errors and single bit glitches. Specifically, the solution automates the process of creating special error detection and correction circuitry. The solution also enables a reproducible, requirements-driven design process from system specification and RTL coding to logic synthesis, verification and the final netlist.

Synopsys Synplify® Premier software incorporates several advanced techniques to detect and mitigate SEUs, which are single-bit radiation induced bitflips that are clocked into a register and, if left uncorrected, have the potential to cause state machine lockup, incorrect design operation or, worse still, operational failure.

For years, designers have been using redundancy in their designs to mitigate radiation-induced soft errors. Synopsys' Synplify Premier software automates these proven methods by allowing the designer to select blocks or registers to be implemented with Triple Module Redundancy (TMR) for error correction. Synplify Premier also automates creation of duplicate with compare double redundant circuitry to flag errors and drive custom mitigation error detection that uses fewer logic resources.

▸ **Distributed TMR**—Synplify Premier software automatically implements user-selected logic in triplicate and adds the associated voting logic to determine the correct state and automatically return the design to correct operation.
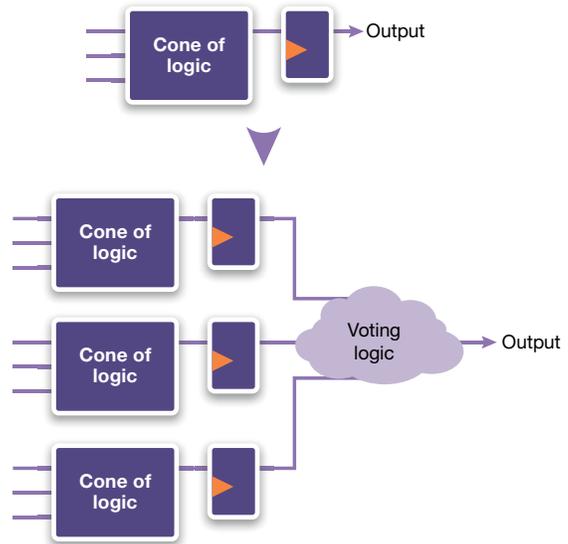
Figure 1: TMR helps mitigate SEUs induced by radiation effects by inserting redundancy during synthesis with triplicated circuitry and voting logic

▸ **Duplicate with Compare Error Detection**—Synplify Premier allows you to automatically create dual-redundant circuitry and comparison logic with an error flag output that provides an alert when the circuitry outputs do not match, thus indicating operational error. This error flag can be used to trigger custom error mitigation, scrubbing, or can act as an error monitor that alerts you to the presence of an error.

▸ **Error Correcting Code (ECC) Memories with TMR**—ECC with TMR can be used for single-bit error detection and correction in memories by preventing false data from being captured in memory and being propagated to other parts of the design.

▸ **Safe State Machine**—Synplify Premier allows you to specify an attribute that tells the tool to use safe state machine encoding algorithms to produce a highly reliable implementation of the state machine in your design. Safe state machines return the design to a safe default state or can perform user-customized error mitigation as specified by an RTL "others" clause.

▸ **Fault-Tolerant FSMs with Hamming-3 Encoding**—In Synplify Premier, users can designate certain FSMs to use Hamming-3 encoding for the automatic detection and correction of single-bit errors.

- **Automated Documentation**—The HDL Analyst tool, built into Synplify Premier, automatically produces highly readable schematics from your HDL source at both the RTL and gate level that may be used for code analysis and professional documentation of your design.

- **Support for Legacy FPGA Devices**—The long life cycles associated with many high-reliability applications demand that design software and FPGA parts be archived for potential future use. Synopsys offers archive licenses of software for this purpose and typically offers synthesis support for mature devices, long after support has been dropped by the FPGA vendor software.

Complete and Accurate Design Specification	✓ Constraints and syntax checking ✓ Design specification checking
Built-in Safety	✓ Triple Modular Redundancy (TMR) automation ✓ Safe Finite State Machines (Safe FSMs) ✓ Duplicate-with-compare error detection ✓ ECC memories ✓ Error monitoring
Debug Chip Operation	✓ Implement and preserve debug logic during synthesis ✓ Generate custom reports and scripts ✓ Debug chip hardware at the RTL level ✓ Develop proof of concept using prototyping hardware/software system
Reproducible, Documented, Portable Design Process	✓ Documentation, archiving and restoration ✓ Support for process compliance for industry specifications ✓ Design portability across FPGA technologies and vendors
Verification and Equivalence Checks	✓ Verification and equivalence checks ✓ Disable optimizations that obstruct requirements tracing

Table 1: The Synplify Premier FPGA Synthesis Tool offers a range of features to enable highly reliable design

Industry Support for Safety Systems

There are many applications being designed today that require high reliability and error mitigation technologies which are driven by industry specific specifications.

Industry standards including DO-254, IEC 61508, and ISO 26262 define functional safety and error mitigation strategies for the creation and validation of high reliability systems. The Synplify family of high-performance, technology-independent implementation and debugging solutions are designed to aid in providing compliant processes for FPGA development in high reliability systems. Accurate functional verification against initial requirements is a critical component of meeting these industry standards. A Synopsys verification flow, using the VCS® RTL verification solution coupled with the techniques outlined in the Verification Methodology Manual (VMM), available for free from the Synopsys website promote the creation, execution, and measurement of a complete verification plan.

The Synplify Premier synthesis tool includes the Identify RTL Debugger, which allows you to instrument RTL HDL and debug the implemented FPGA design on the hardware. The software verifies a design in hardware, similar to simulation but allowing the designer to find errors that would take weeks to find with simulation. The software allows designers to designate sample triggers, navigate the design graphically, and mark signals in the RTL to serve as probes. After synthesis, the results of running test vectors through the design can be viewed and annotated onto the RTL source code, the HDL Analyst® RTL View, or third party waveform viewer for easy visualization and debug of design operation.

RTL Verification, Proof-of-Concept Development, and FPGA-Based Design

Synopsys offers the VCS functional verification and debug environment, enabling chip and system developers to find and fix critical design defects as early as possible to avoid schedule delays and keep production costs to a minimum. VCS, along with the VMM methodology, support a high reliability compliant RTL verification solution. The Synplify tools provide the fastest time to first hardware and software integration which accelerates the customer's development schedule. Software development and system validation teams will benefit from improved productivity and a reduction in the overall product development schedule. The complete solution consists of the integrated tool flow including Synplify Premier FPGA synthesis software and the Identify® RTL Debugger. The integrated tool flow seamlessly integrates with Synopsys' HAPS FPGA-based prototyping platform, which is ideal for demanding validation environments. The system can be used for the creation of end product systems, for algorithm development and for the development and validation of high quality IP where real-world interfaces and large test suites are essential.

Solutions for High-Throughput Signal Processing

Implementing complex signal processing solutions requires a sophisticated design and test methodology to ensure robust operation of integrated products. In addition, the ability to re-use design and verification data across multiple FPGA technology targets (FPGA and ASIC) can significantly reduce effort, schedule, and risk for signal processing FPGA designs. Synopsys provides complete solutions for vendor-independent signal processing design, including:

▶ Synopsys signal processing IP for fast design implementation
▶ High-level design and verification from MATLAB/Simulink® environment
▶ Fast simulation technologies including C models for fixed-point verification, system validation, multi-domain simulation
▶ Fast RTL synthesis turnaround for architecture exploration
▶ Superior quality of results across FPGA and ASIC
▶ World-wide support for algorithm, IP, and hardware design

With Synopsys' Synphony Model™ Compiler signal processing solution, customers have achieved orders of magnitude higher productivity while maintaining a vendor-independent design and verification methodology. Furthermore, customers benefit from the expertise of a world-wide Synopsys support team that can support all levels of the design flow including algorithm design, signal processing IP, logic synthesis, and overall quality of results.

For more information on the Synopsys FPGA design solution visit http://www.synopsys.com/Tools/Implementation/FPGAImplementation/FPGASynthesis/Pages/HighReliability.aspx.