SYNOPSYS®

DATASHEET

DFTMAX Ultra

Compression for Highest Test Quality and Lowest Test Cost

Addresses the most demanding test cost and quality requirements, enabling higher compression and faster test frequencies using fewer test pins

Overview

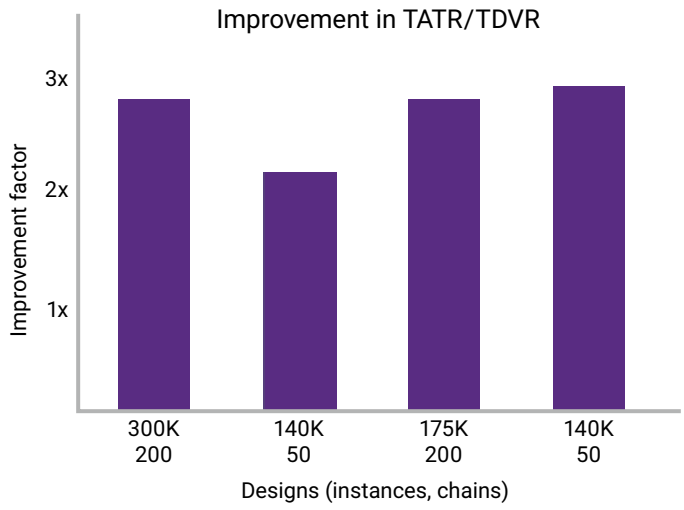
DFTMAX™ Ultra addresses the most demanding test quality and test cost requirements with innovative synthesis-based technology that enables higher compression and faster test frequencies using fewer test pins. Encapsulated in Synopsys' Galaxy™ Implementation Platform, DFTMAX Ultra works seamlessly with TetraMAX® ATPG to predictably achieve high defect coverage and accurate fault diagnostics without adversely impacting design goals and schedules.

Key Benefits

- Significantly lowers manufacturing test costs
- Enables higher defect coverage of silicon parts
- Utilizes the maximum performance of tester equipment to further reduce test time/cost
- Minimizes the required number of scan I/O for pin-limited testing
- Provides simplified and fast test implementation

Key Features

- 2-3x higher compression:
  - Bidirectional compressor-decompressor (CODEC) for simultaneous streaming and de/compression of test data
  - Built-in X-tolerance for high fault coverage, efficient compression, and accurate diagnostics
  - Pipelined processing enables high-speed shifting for 4-6x further test time/cost reduction
- Architecture utilizes as few as one scan channel for pin-limited test
- Non-gated CODEC and scan clocking eliminates the need for external clock controllers, simplifies implementation
- Seamless integration with TetraMAX for high defect-coverage testing and power-aware testing
- Works in conjunction with DesignWare® STAR Hierarchical System for hierarchical test of systems-on-chip (SoCs)
- Built into Synopsys' Design Compiler RTL synthesis for concurrent optimization of timing, power, area, physical, and test constraints
- Encapsulated in Synopsys' Galaxy Implementation Platform for faster turnaround time meeting both design and test goals



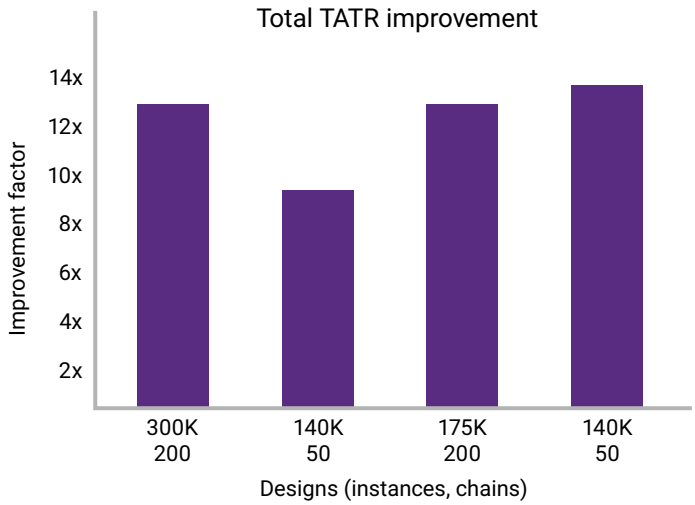
Source: Synopsys customer design suite

Figure 1: DFTMAX Ultra improves TATR/TDVR by 2-3x compared with standard low pin count architectures. Each design shown uses a single scan channel for compression

Higher Compression for Lower Cost and Lower DPPM

As SoCs increase in gate count and complexity, more test data is needed to achieve high fault coverage, which increases compression levels required to maintain low test costs. Also, on-chip process variations give rise to subtle fault effects that require application of additional high defect-coverage tests that complement stuck-at and transition delay tests to cover the associated defects. These additional tests—slack-based transition delay tests, static/dynamic bridging tests, etc.—enable the lowest defective parts per million (DPPM) at both established and advanced process nodes but increase test execution time and data, further driving up test application time reduction (TATR) and test data volume reduction (TDVR) requirements.

DFTMAX Ultra delivers 2-3x higher compression to address the more demanding TATR/TDVR requirements of large SoCs and high defect-coverage testing. It accomplishes this using a bidirectional CODEC that enables simultaneous streaming and de/compression of test data, thereby eliminating pipeline stalls between scan shifts that occur in standard serial-deserialization (SERDES) implementations. The architecture also provides TetraMAX with maximum flexibility to target faults and manage unknown logic values (Xs). Built-in X-tolerance improves test coverage, increases compression efficiency, and facilitates accurate fault diagnostics. The chart in Figure 1 shows the improvement in TATR/TDVR for several customer designs.



Source: Synopsys customer design suite

Figure 2: Total TATR improvement for the designs of Figure 1 when the tester clock frequency was increased from 10 MHz to 60 MHz. DFTMAX Ultra enables high-speed shtifting of test data to further lower test time/cost

Faster Scan Operations for Further Reduction in Test Time and Cost

TATR levels can be improved further by scanning test data in and out of designs faster, using a higher tester clock frequency to increase the rate at which internal scan chains are shifted. Pipelined processing of all data in and out of the DFTMAX Ultra CODEC facilitates high-speed shifting of the test data, making it possible to utilize the maximum performance of tester equipment to further reduce test application time and cost by a factor of 4-6x. The chart in Figure 2 shows the total improvement in TATR for the designs of Figure 1 when the tester clock frequency was increased from 10 MHz to 60 MHz.

High Compression for Pin-Limited Test

The demand for pin-limited compression is being driven by an increased focus on packaging costs and tighter form factors, the design of multicore SoCs that allow few pins per core for test access, and the adoption of multisite testing as a technique to reduce test application time and cost. DFTMAX Ultra's architecture is designed from the ground up to achieve high compression using fewer scan channels and a minimum of one scan channel.

Easy to Deploy and Use

DFTMAX Ultra makes it even easier to implement compression and achieve predictable results. The tool requires just two basic parameters: the number of scan chains and the number of scan channels. It then selects the appropriate integration methodology (i.e., top-down, bottom-up, or hybrid) and the architectural variants needed to produce the highest possible fault coverage and compression results. Since the CODEC uses the same clocking as the scan chains, there is no need for external clock controllers and glue logic for test, further simplifying DFT implementation and minimizing its impact on design schedules.

Value Links for Higher Test Quality and Faster Turnaround Time

DFTMAX Ultra is seamlessly integrated with TetraMAX ATPG and TetraMAX DSMTest to predictably achieve high compression and high test coverage for standard, high defect-coverage, and power-aware testing. DFTMAX Ultra and TetraMAX are part of Synopsys' synthesis-based test solution, which also includes DesignWare STAR Hierarchical System for IEEE standards-based hierarchical SoC test; DesignWare STAR Memory System® for embedded and external memory test, repair, and diagnostics; DesignWare IP for high-speed interfaces with self-test; Yield Explorer for design-centric yield analysis; and Camelot™ for CAD navigation.

Synopsys' test solution combines Design Compiler RTL synthesis with embedded test technology to optimize timing, power, area, and congestion for test as well as functional logic, leading to faster time-to-results due to zero or minimal design iterations. The solution contains value links among the test products and across the Synopsys Galaxy™ Implementation Platform to enable faster turnaround time meeting both design and test goals, higher defect coverage, and faster yield ramp.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.