SYNOPSYS®
Silicon to Software™

DFTMAX LogicBIST

Synthesis-Based In-System Self-Test

Overview

DFTMAX™ LogicBIST is a synthesis-based solution for in-system self-test of digital integrated circuits used in automotive, medical and aerospace applications. Built into Design Compiler® for concurrent optimization of area, power, timing, physical and test constraints, DFTMAX LogicBIST enables design teams to converge quickly on quality, cost goals, and functional safety requirements set forth by standards such as ISO 26262 for the automotive semiconductor industry.

Key Benefits

- Addresses in-system self-testing requirements, including ISO 26262 functional safety
- Predictably achieves target test coverage within given run time, clock frequency, and power constraints
- Maximizes designer productivity by utilizing value links across the Galaxy™ Design Platform
- Complements DFTMAX for scan-based manufacturing test
- Requires minimal silicon area

Key Features

- Built into Design Compiler
- High fault coverage with pseudo-random patterns and test points
- Optimized for applications with limited number of interface pins
- Go/no-go response derived from on-chip seed and signature
- Optional IEEE 1500 interface and activation
- User-specified operational runtime

In-System Logic Self-Test for ISO 26262 Functional Safety

With the rapid growth of sophisticated automotive instrumentation, a typical car today relies on electronics for controlling safety-critical components such as engine, transmission, air bags, steering, and braking system. As the corresponding ICs are stressed by temperatures, power fluctuations, humidity, vibration, and aging throughout their life cycle, automotive IC suppliers intensively focus on silicon quality and reliability. Indeed, safety-critical devices in the system must be able to routinely perform self-test in compliance with the ISO 26262 automotive functional safety standard, verifying that the circuitry operates without structural defects.

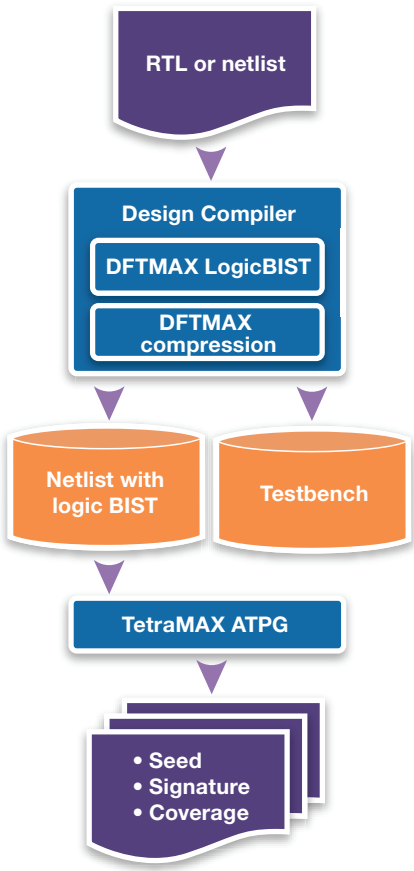

Figure 1: Synopsys synthesis-based logic BIST flow

To address this requirement, DFTMAX LogicBIST synthesizes on-chip circuitry that enables quick in-system testing.

Fast Turnaround Time

Synopsys' test solution combines Design Compiler RTL synthesis with embedded test technology to optimize for timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results.

To further simplify design-for-test (DFT) implementation and minimize its impact on design schedules, DFTMAX LogicBIST works in conjunction with DFTMAX compression and TetraMAX® ATPG to provide test point analysis and insertion, seed and signature computation, coverage calculation, and engineering change order (ECO) management (Figure 1).

For fast ramp-up DFTMAX LogicBIST uses familiar commands, configuration settings, and customization capabilities. To meet system-level requirements, designers can adjust various BIST engine specifications to balance the area impact, operational run time, and other goals. Furthermore, options exist to add functionality for burn-in testing.

Simple, Minimal Interface

The DFTMAX LogicBIST interface is optimized for applications with a limited number of interface signals, making it ideal for small and mixed-signal automotive designs that need to quickly identify potential safety issues and send error codes to the vehicle's processing system. For example, the self-test is initiated by simply holding the START signal high. If no error is detected, the PASS/FAIL output will be low. One additional signal DONE completes the entire interface (Figure 2).

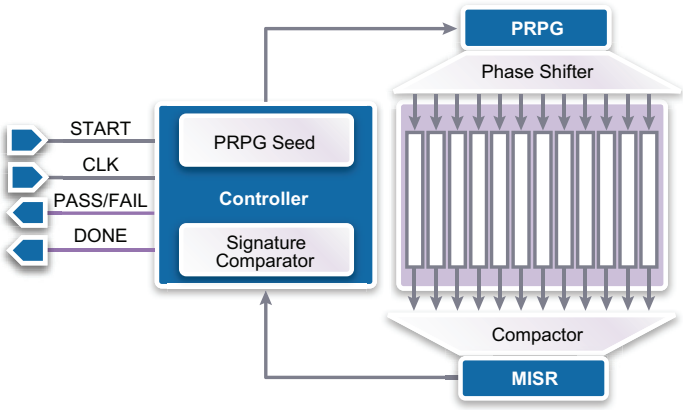

Figure 2: DFTMAX LogicBIST architecture

SoC-Level Integration

Design Compiler synthesizes logic BIST, scan, and compression for manufacturing test as well. These DFT structures are automatically integrated into the top-level architecture using DFTMAX. To accommodate hierarchical test, DFTMAX supports connection of the logic BIST to IEEE 1500 test infrastructure, enabling chip-level access through the standard IEEE 1149.1 interface.

Highest Quality and Lowest Cost Manufacturing Test

In addition to implementing in-system logic BIST, designers of automotive and other mission-critical ICs must also achieve stringent manufacturing test quality and cost goals. To achieve the highest quality levels, typically less than one defective part per million (DPPM), TetraMAX ATPG generates manufacturing tests targeting various silicon defects using state-of-the-art fault models that incorporate the designs' timing and physical characteristics. To minimize test time and cost for pin-limited and mixed-signal designs, DFTMAX Ultra synthesizes test compression circuitry, utilizing as few as one scan channel.

Synopsys Synthesis-Based Test Solution

DFTMAX LogicBIST provides in-system self-test and predictably achieves high defect coverage. It is a part of Synopsys' synthesis-based test solution which also includes DFTMAX, DFTMAX Ultra, and TetraMAX for power-aware manufacturing test and physical diagnostics; the DesignWare® STAR Hierarchical System for hierarchical test of IP and cores on an SoC; DesignWare STAR Memory System® for embedded test, repair, and diagnostics; the Yield Explorer® tool for design-centric yield analysis; and the Camelot™ software system for CAD navigation. The Synopsys test solution delivers tight integration across the Synopsys Galaxy Design Platform, including Design Compiler, IC Compiler™ II and PrimeTime®, to enable faster turnaround time meeting both design and test goals, higher defect coverage and faster yield ramp.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.

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