SYNOPSYS®
Silicon to Software™

High Quality, Low Cost Test

Overview

DFTMAX™ is a comprehensive synthesis-based test solution for compression and advanced design-for-test that addresses the cost challenges of testing complex designs. Designs can have subtle manufacturing defects that are only detected by applying high defect-coverage tests, such as at-speed and bridging tests, in addition to stuck-at tests. The extra patterns needed to achieve high test quality for these designs can increase both the test time and the test data, resulting in higher test costs.

DFTMAX reduces these costs by delivering push-button high test data and test time compression with very low silicon area overhead. Seamlessly enabling compression in TetraMAX® ATPG, and encapsulated in Synopsys' Galaxy™ Design Platform, DFTMAX achieves predictable results with virtually zero impact on timing. The DFTMAX Ultra add-on to DFTMAX addresses the need for ever-higher compression using fewer test pins.

Key Benefits

- Lowers test costs
- Enables high defect coverage
- As easy-to-use as standard scan
- Avoids any impact on design timing
- Leverages physical design for area optimization
- Preserves low-power design intent
- Minimizes power consumption during test
- Works in conjunction with SpyGlass DFT® ADV, the DesignWare STAR Memory System and DesignWare STAR Hierarchical System

Key Features

- High test time and test data reduction (typical)
- Based on patented, powerful DFTMAX compression technology
- Built into synthesis and ATPG—easy to implement as standard scan
- Multicore compute platform support
- Integrated with Design Compiler® and IC Compiler for concurrent optimization of area, power, timing, physical and test constraints
- Comprehensive test DRC analysis
- Hierarchical scan synthesis flow support
- Pin-limited test optimizations
- Unknown logic value (X) handling
- Location-aware scan chain reordering during incremental compile
- Core wrapping with shared use of existing core registers near core I/Os
- Analysis-driven test point insertion using SpyGlass DFT ADV
- Flexible scan channel configurations to support multi-site testing and wafer-level burn-in
- Multiple compression configurations to support different testers and packages with different I/O
- Boundary scan synthesis, 1149.1/6 compliance checking and BSDL generation
- Enables TetraMAX ATPG for compressed pattern generation

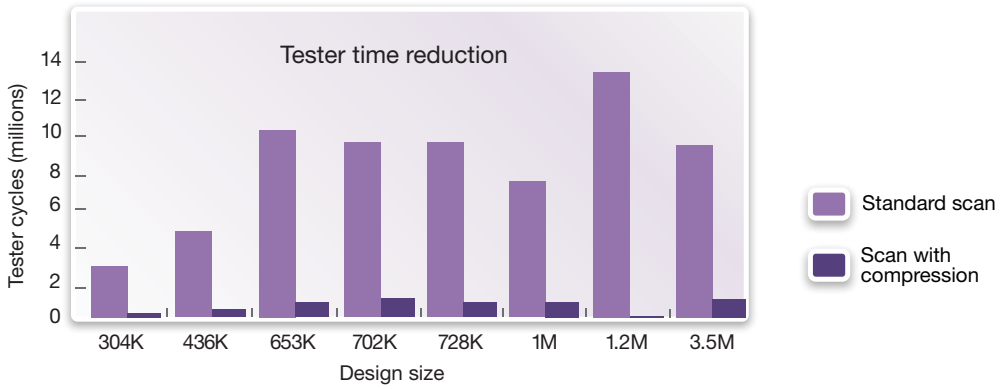

Figure 1. DFTMAX delivers high test time and test volume reduction

DFTMAX Delivers High Test Time and Test Volume Reduction

DFTMAX reduces the costs of nanometer testing by providing high test data volume compression (Figure1). Using Synopsys' patented DFTMAX compression architecture, DFTMAX saves test time and makes it possible to include high defect-coverage test patterns in tester configurations where memory is limited. With the industry's most area-efficient solution, DFTMAX has virtually no impact on design timing and results in the same high test coverage as provided by standard scan (Figure 2a).

Pin-Limited Test

To accommodate designs that require a limited number of test data pins either at the top-level or per core, DFTMAX generates an optimized architecture that ensures high quality without incurring extra test data. Several current trends that are limiting the number of available test pins include tighter form factors, multi-site testing to target multiple die simultaneously, and core-based methodologies with multiple embedded compressor-decompressors (CODECs). These types of techniques minimize the number of chip-level test pins available to each CODEC. To provide high test data volume and test application time reduction for these pin-limited test applications, DFTMAX generates a high-speed, low-pin tester interface that automatically serializes the test data. Use DFTMAX Ultra to minimize the required number of scan I/O for pin-limited testing (Figure 2b).

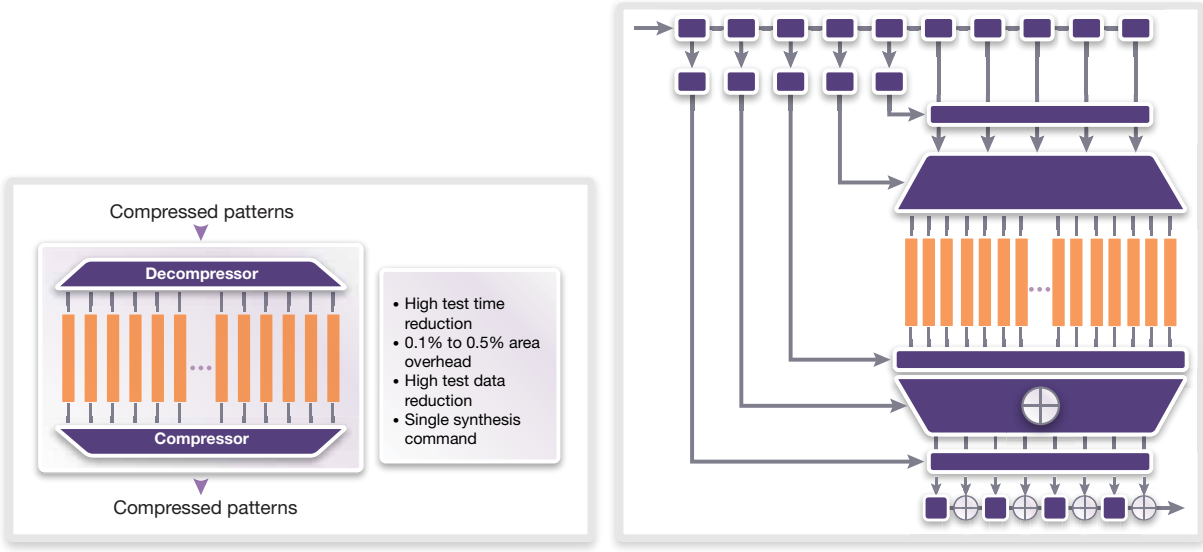

Figure 2a. (left) DFTMAX,
Figure 2b. (right) DFTMAX Ultra minimizes the required number of scan I/O for pin-limited testing

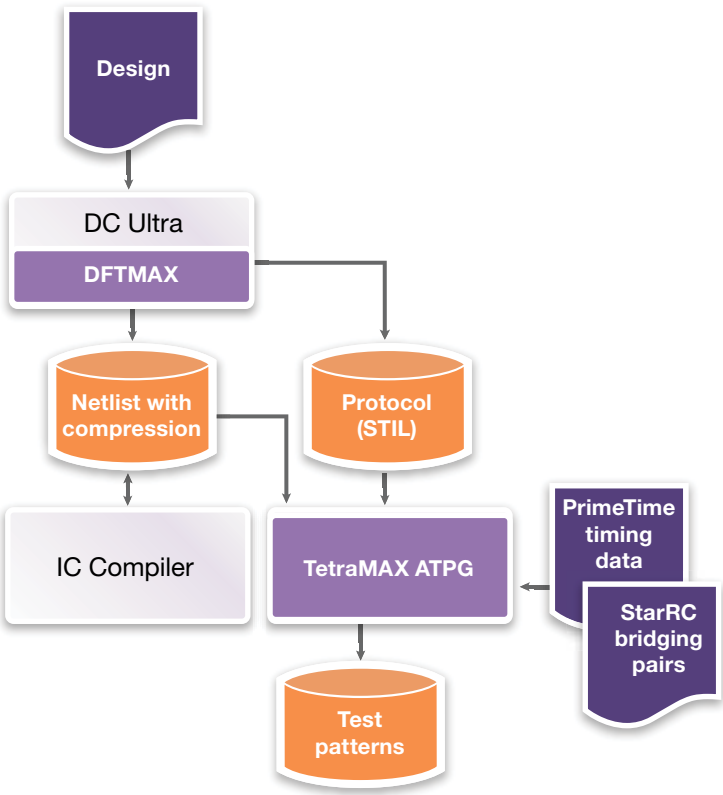

Figure 3. Test compression flow

Test Compression Synthesis

The DFTMAX synthesis flow is practically the same as the industry's most widely deployed standard scan synthesis flow enabled by DFT Compiler. DFTMAX synthesizes test compression directly from RTL to testable gates with full optimization of synthesis design rules and constraints. All test and compression requirements specified prior to the synthesis process are met concurrently with area, timing and power optimization. DFTMAX synthesizes the design at the gate-level with all scan design rules checked and the test and compression logic verified, leading to very high and predictable test coverage and test compression results. The implementation of DFT, including test compression, within the design synthesis environment allows problems to be found and fixed earlier in the design cycle, thus avoiding 'schedule-breaking' design iterations. DFTMAX also enables TetraMAX ATPG to seamlessly generate compressed test patterns having the highest test quality.

Integration With Galaxy Design Platform For Concurrent Optimization Of Area, Power, Timing, Physical And Test Constraints

With Synopsys' unique synthesis flow (Figure 3), scan compression logic is synthesized simultaneously with scan chains within the Galaxy Design Platform. Topographical scan chain ordering and partitioning provides excellent timing and area correlation with physical results using IC Compiler. This enables designers to achieve area, power, timing and DFT closure simultaneously. DFTMAX writes detailed scan chain information which IC Compiler then reads to perform further optimizations to reduce area impact and decrease overall routing congestion (Figure 4).

Integrating DFT resources into a complex multi-voltage design can be a time-consuming and error-prone process without automation tailored for low-power flows. Once voltage domain characteristics of the design with IEEE 1801 (unified power format) are specified, DFTMAX automatically inserts level shifters and isolation cells during scan chain implementation. To reduce routing congestion and area impact of the DFT logic, DFTMAX minimizes both scan chain crossings between power/voltage domains and the number of level shifters inserted.

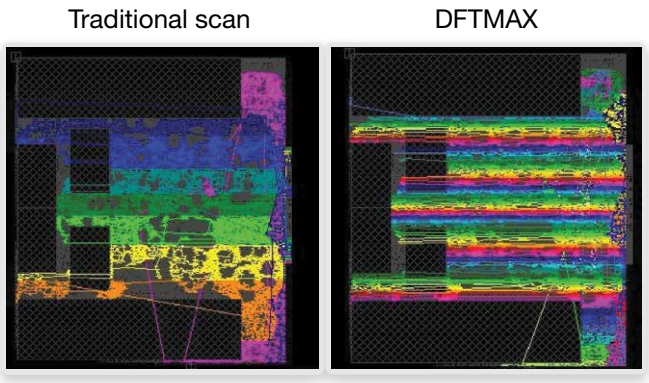

Figure 4. These screen captures show DFTMAX results without the routing congestion associated with standard scan

Complete DFT Rules Checking

For maximum productivity, and prior to executing DFTMAX, SpyGlass DFT ADV enables designers to create "test-friendly" RTL. It identifies DFT rules violations early in the design cycle during the pre-synthesis stage to avoid design iterations. SpyGlass DFT ADV validates that the design is compliant with scan rules to ensure operational scan chains and the highest test coverage. The violations can be diagnosed using its powerful integrated debugging environment that enables cross-probing among violations, RTL and schematic views. SpyGlass DFT ADV has comprehensive rules checks for:

- Violations that prevent proper scan operation
- Violations that lower fault coverage
- Hard-to-test faults that increase pattern counts

The DRC engines are consistent from RTL to gate level, making it possible for designers to validate testability all the way through the design synthesis process.

Hierarchical Scan Synthesis

To handle test synthesis of very large designs, some level of abstraction is required so that the system/chip integrator can reduce design time. By abstracting the DFT information in a test model, along with timing and placement information, DFTMAX enables quick hierarchical test implementation of multi-million gate designs.

Boundary Scan Synthesis and Compliance Checking to the 1149.1/6 Standard

DFTMAX delivers a complete set of boundary scan capabilities including:

- TAP and BSR synthesis
- Compliance checking to the IEEE 1149.1/6 standard
- Boundary Scan Description Language (BSDL) file generation
- Functional and DC parametric pattern generation for manufacturing test

Transparent Integration in TetraMAX ATPG for Power- Aware Test

DFTMAX transfers all information about the scan compression architecture and test operation to TetraMAX ATPG. Working together, TetraMAX ATPG and DFTMAX automatically generate compressed, power-aware test patterns with highest test coverage.

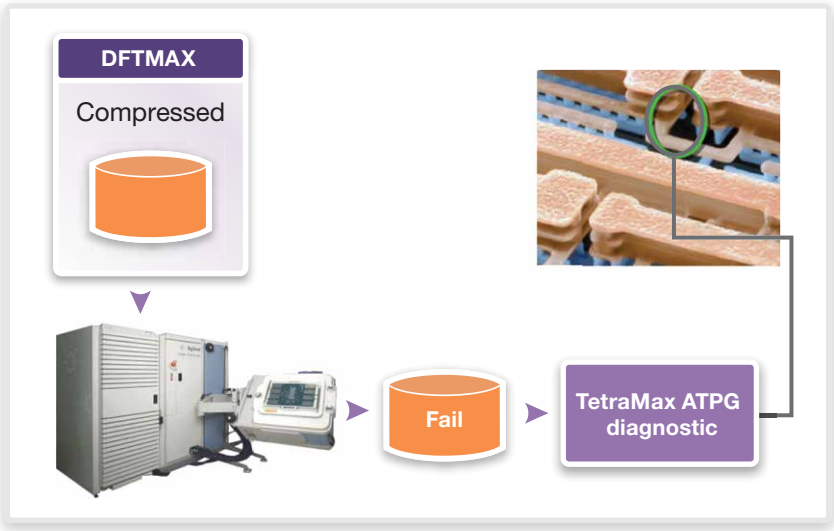

Figure 5. DFTMAX fully supports proven TetraMAX ATPG ATE links for an effective and accurate yield diagnostic solution

Integration With TetraMAX ATPG Diagnostics

DFTMAX fully supports proven TetraMAX ATPG ATE links for failure diagnosis and delivers a straightforward flow from tester fail to location of the defect. DFTMAX and TetraMAX ATPG diagnostics together deliver a very effective and accurate yield diagnostics solution (Figure 5). For fast resolution of yield issues, the diagnostics data from TetraMAX ATPG can be automatically read and analyzed by the Yield Explorer yield management system.

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