SYNOPSYS®

DATASHEET

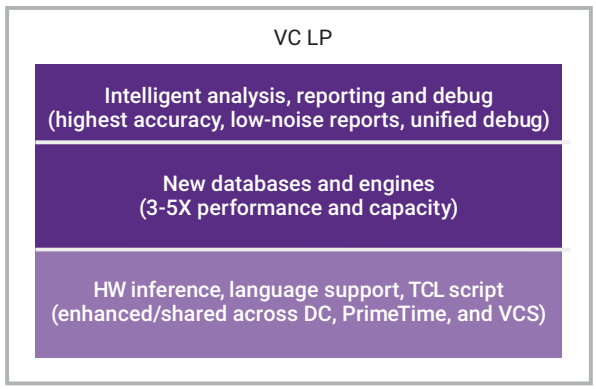
VC LP

Next-Generation Low Power Static Checking

Validate UPF low power design intent is accurately implemented and functions correctly

Overview

SoC designs use low power design techniques to enable support for advanced power management required in many of today's electronic products, from mobile device to servers and networking. Advanced low power techniques such as Power Gating, Retention, Low-Vdd Standby, and Dynamic Voltage Scaling (DVS) employ voltage control to enable fine-grained power management, and are seeing increasingly prevalent adoption. Due to the nature of low power design architectures and behavior, low power verification complexity is exponentially more challenging than for always-on verification. Native low power simulation and advanced low power static verification and signoff must manage this increased complexity, and still attain all verification objectives.



Static Checking Challenges for Low Power Designs

Advanced intent-driven low power design flows requires complete and rapid checking of low power implementation and behavior validity at every stage in the flow. In addition, analyzing, debugging and fixing violations must be easy and efficient, in order to effectively enable designers to eliminate possibly design-killing low power bugs early in the design flow.

Low power SoC designs are partitioned into power domains that can be separately controlled by one or more low power design techniques, and verification complexity increases exponentially with the number of power domains. Also, increasingly stringent power requirements have necessitated the use of multiple supply voltages, adding another dimension to verification complexity. Finally, low power designs typically operate in multiple modes, with each mode corresponding to one or more power states—yet a third dimension of additional complexity. Comprehensive verification of low power designs requires verification not just in all the power domains, all combinations of supply voltages, and all power states and modes, but also of the specified transitions and transition order within these power states as the design moves from one operating mode to another. A single bug in any of these incredibly complex scenarios may cause functional failures in silicon.

Low power design techniques add new design elements at different stages of the design flow. Architectural design bugs that violate the principles of low power design may exist even at RTL. Isolation cells are typically synthesized automatically. Retention register connections need to be validated after synthesis and again after place and route. Multi-voltage designs require the appropriate power and ground pins to be connected to the specified supply rails. Low power static checking must operate comprehensively in all stages of the design flow in order to accurately verify correct implementation and behavior in all of these cases.

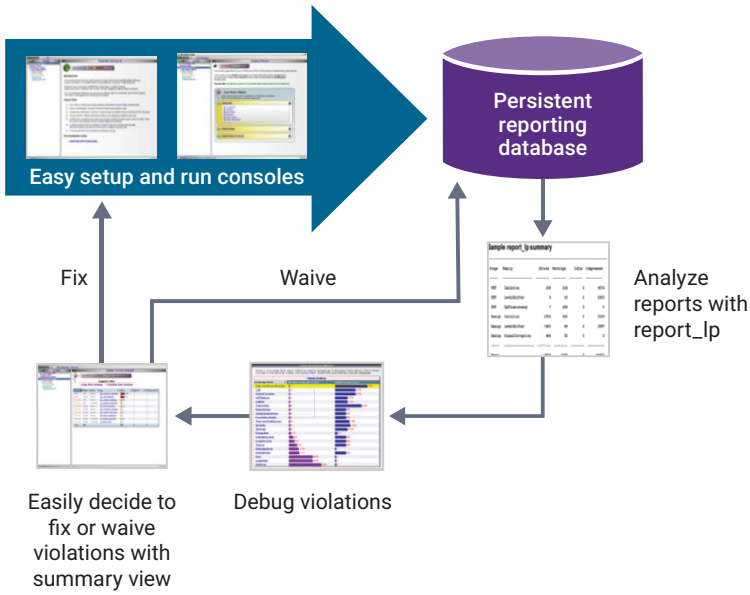


Figure 1: VC LP checking, reporting and waiving flow

VC LP

VC LP is a multi-voltage low power static rule checker that can help pipe-clean IEEE 1801 Unified Power Format (UPF) low power design intent, and validate that UPF low power design intent is accurately implemented and functions correctly. VC LP provides extensive reporting, filtering and waiving capabilities to simplify and expedite even the most complex low power verification signoff flows. VC LP provides efficient and effective low power debug capabilities. Design load and setup needs to be only done once for any or all of the three products, and all three share similar usability, reporting and debug features.

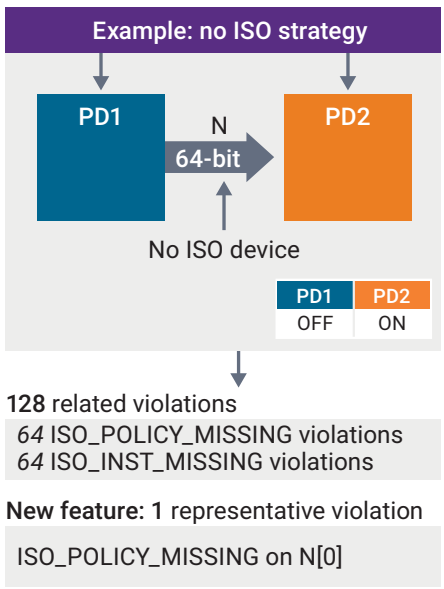


Figure 2: Violation compression

Key Features and Benefits

- **Power Intent Consistency Checks:** Syntax and semantic checks on UPF that help validate the consistency of UPF prior to implementation. Incorrect power intent will result in incorrect low power design implementation. The UPF consistency checks ensure that the power intent specification driving low power implementation is syntactically and semantically correct
- **Architectural Checks:** Global checks at RTL for signals violating power architecture rules. VC LP validates the design in its entirety and checks the critical signal networks in the design for the various power modes. These checks help find connectivity related bugs, which would cause functional issues very early in the design cycle
- **Structural and Power and Ground (PG) Checks:** Validation of insertion and connection of isolation cells, power switches, level shifters, retention registers and always-on cells throughout the implementation flow, from initial synthesis to place and route (See Figure 2)
- **Functional Checks:** Checks the correct functionality of isolation cells and power switches. The most accurate and production-proven support for industry-standard IEEE 1801 Unified Power Format (UPF) power intent
- **Hierarchical Power State Analysis:** Designs with a large number of power domains benefit from the automatic derivation of a hierarchical power- state table. VC LP understands the power intent and is able to prune a large number of power states to a few distinct ones, thus reducing the effort involved to specify and then verify all the power states, transitions and sequences
- **Complex Power State Table Debug:** Related to hierarchical power state analysis, VC LP provides users the ability to understand and if necessary, debug the resulting complex power state tables

```
> set BM_ROOT /remote/vgbench7/benchmarks/TOP_GATE_MVRC_SNPS

> set search_path "$BM_ROOT $BM_ROOT/LIBS $BM_ROOT/2_dbs"

> set link_library  "*
C32_IO_SF_C2C_PROG1V21V8_LR_EG_5U1X2T8XLB_ss32_0.95V_125C.db \
C32_IO_SF_COMPENSATION1V2_LATCH_LR_EG_5U1X2T8XLB_ss_0.90V_1.08V_125C.db \ ..."

> read_file -format verilog -top chip -netlist "chip_top.PostSyn.v"

> read_upf chip_top.PostSyn.upf

> check_upf      # Validating UPF

> check_design # Validating design

> report_lp    # extract violations from database

> quit
```

Figure 3: Design Compiler/IC Compiler-like scripting

Unique Values

- **Industry-leading performance and capacity**
  - Ability to efficiently run on the largest SoC designs at both RTL and netlist levels. At least 3X-5X faster and higher capacity than other tools
- **Excellent ease of adoption and ease-of-use**
  - Use model and commands tightly aligned with Synopsys' implementation tools
  - VC LP not only supports all Design Compiler® TCL query commands, but also provides unique TCL query/debug commands for low power objects in the design
  - Designers can use these query commands to write custom checks (See Figure 3)
- **Reporting filtering and waivers**
  - Highly flexible tag- and message-based filtering and waiving capabilities for rapid and effective low power verification signoff flows (See Figure 1)
- **Powerful low power-optimized debug**
  - GUI-based low power debugging with powerful schematic features such as locators to identify key low power objects, ability to add custom labels for debugging complex schematic paths, and property windows to inspect details of any object on the schematic
  - All violation messages can be cross-probed with UPF, schematic and source code views
  - VC LP is also integrated with Verdi for low power-specific visual guidance, including box-in-box representation of hierarchical instances (See Figure 4)

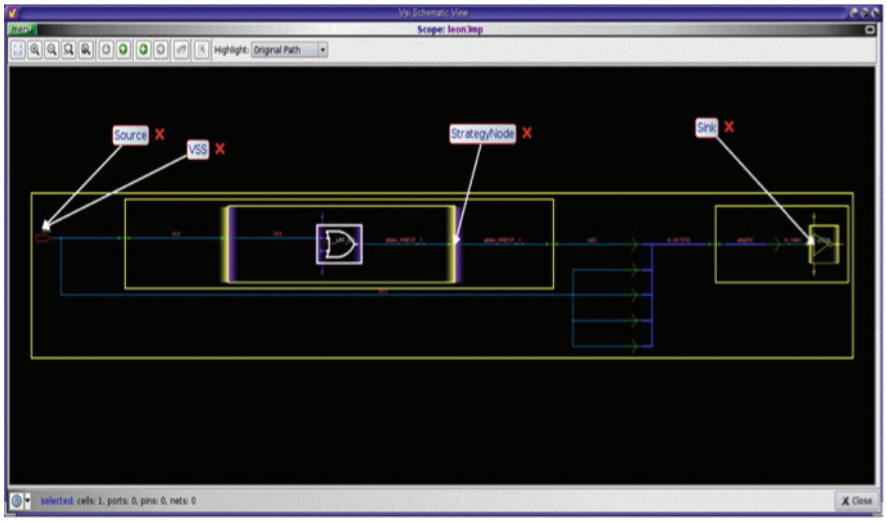


Figure 4: VC LP's box-in-box schematic view

Conclusion

Adoption of advanced low power design techniques is growing rapidly to support ever-more sophisticated system level power management schemes. Fine-grained voltage control-based low power design techniques require stringent validation and checking throughout implementation and verification flows. VC LP's comprehensive and accurate low power static rule checks understand the most complex power intent and has the capacity and performance for the largest SoC designs. VC LP is in production deployment and adopted at industry-leading customers.

For more information about Synopsys products, support services or training, visit us on the web at: synopsys.com