Synopsys Learning Paths
A guide to your learning journey
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## Custom Compiler Learning Path: Analog Designer

### Course 1: CC: Foundation I
- Custom Compiler Overview
- Library Manager
- Data I/O
- Technology
- Design Review Assistant
- Unified Constraint Management
- Capturing Schematics
- Using Advanced Editing features
- Generating Symbols
- Schematic Entry
- Advanced Schematic Editing
- Symbol Creation
- Design Hierarchy
- Working with Text Views
- Parameterized Connections
- Schematic Overlays
- Using Estimated Parasitic

### Course 2: CC: Schematic Entry
- Capturing Schematics
- Using Advanced Editing features
- Generating Symbols
- Schematic Entry
- Advanced Schematic Editing
- Symbol Creation
- Design Hierarchy
- Working with Text Views
- Parameterized Connections
- Schematic Overlays
- Using Estimated Parasitic

### Course 3: PrimeWave Jumpstart
- Capturing Schematics
- Using Advanced Editing features
- Generating Symbols
- Schematic Entry
- Advanced Schematic Editing
- Symbol Creation
- Design Hierarchy
- Working with Text Views
- Parameterized Connections
- Schematic Overlays
- Using Estimated Parasitic

### Course 4: PrimeWave & PrimeSIM SPICE Analog Tutorial
- Testbench Setup
- Parametric Analysis
- Corner Analysis
- Monte Carlo Analysis
- Dynamic Device Checks
- Symbol Creation
- Design Hierarchy
- Working with Text Views
- Parameterized Connections
- Schematic Overlays
- Using Estimated Parasitic

### Course 5: CC: Reliability
- OP, DC, Tran Analysis
- Parametric Analysis
- Corner Analysis
- Monte Carlo Analysis
- Dynamic Device Checks
- Symbol Creation
- Design Hierarchy
- Working with Text Views
- Parameterized Connections
- Schematic Overlays
- Using Estimated Parasitic

### Legend
- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge
Custom Compiler Learning Path RF/Transceiver Designer

**Course 1: CC: Foundation I**
- Custom Compiler Overview
- Library Manager
- Data I/O
- Technology
- Design Review Assistant
- Unified Constraint Management

**Course 2: CC: Basic Layout Design**
- Layout Design Entry
- Abutment & Align Functions
- Advanced Editing Functions
- Hierarchical Design Creation
- Connectivity Engine
- Abstract Generation
- Design Rule Aware Editing
- Mcell Guard Ring
- Advanced Node Support
- Multi Pattern Technology
- User Defined Devices (UDD)
- Physical Verification
- Parasitic Extraction

**Course 3: CC: Accelerated Layout Design**
- Schematic Driven Layout (SDL) Initialization
- SDL Placement with Connectivity Use
- SDL ECO & Cross Object Referencing
- Placement Advanced
- Symbolic Editor
- Visually Assisted Automation
- Template Manager

**Course 4: CC: Reliability**
- PrimeSim ResCheck Analysis
- PrimeSim EMIR Reliability Analysis
- In-Design EM Aware Layout Implementation
- In-Design Capacitance Reporting
- In-Design Resistance Checking and Reporting
- Partial Layout Extraction (needs CC Elite license)
- Layout Dependent Effects
- Voltage Dependent Rule Check

**Course 5: CC: Automated Layout Design**
- Placement Assistant
- Pin Placer
- Block Placer
- Router Introduction
- Pattern Router
- Interactive Router
- Auto Router
- Shielding
- Scripting
- Antenna Rule Support
- Technology Enablement

Legend:
- Self-paced Learning
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- Downloadable Lab
- Cloud-based Lab
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- Badge
Custom Compiler Learning Path **RF/Transceiver Designer**

Course 6

CC: ICC2 CoDesign

- Data Preparation
- Analog BlackBox Preparation
- Digital Implementation
- ICC2 Editing
- Capacitance Reporting and Checking

Legend:
- Self-paced Learning
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- Downloadable Lab
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Custom Compiler Learning Path **CAD Engineer**

**Course 1**
- CC: Foundation I
  - Custom Compiler Overview
  - Library Manager
  - Data I/O
  - Technology
  - Design Review Assistant
  - Unified Constraint Management

**Course 2**
- CC: Foundation II
  - Tcl API
  - Customization
  - Dialog Boxes
  - Obtaining Database Information
  - User Commands
  - User Interface
  - Creating Effective Tcl Scripts
  - Design Migration
  - Component Description Format (CDF)
  - Performance Monitor
  - Customizing the Netlister
  - PDK Setup (for SDL)

**Legend**
- Self-paced Learning
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- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge
## Design Compiler NXT Learning Path

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<th>Course 1</th>
<th>Course 2</th>
<th>Course 3</th>
<th>Course 4</th>
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</thead>
<tbody>
<tr>
<td>DC: Jumpstart</td>
<td>DC: Synthesis NXT</td>
<td>DC: DFT Insertion</td>
<td>DC: SystemVerilog for RTL Design</td>
</tr>
</tbody>
</table>

**Course 1: Introduction**
- Introduction
- Design Setup
- Reading RTL Design
- Loading Floorplan Data
- Constraining Design
- Synthesis Techniques
- Post Synthesis Outputs

**Course 2: DC: Synthesis NXT**
- Introduction to DC NXT
- Design Setup for Physical Synthesis
- Accessing Design and Library Object
- Constraints: Reg-to-Reg and I/O Timing
- Advanced Schematic Editing
- Input Transition and Output Loading
- DC NXT Ultra Synthesis Techniques
- Timing Analysis
- Constraints: Multiple Clocks and Exceptions
- SPG Flow: Congestion, Layout GUI
- Constraints: Complex Design Considerations
- Post-Synthesis Output Data
- Ck Gating/Leakage Power analysis

**Course 3: DC: DFT Insertion**
- Introduction
- Scan Testing and Flows
- Test Protocol
- DFT Design Rule Checks
- DFT DRC GUI Debug
- DRC Fixing
- Top-Down Scan Insertion
- Advanced Scan Insertion
- Bottom-up Scan Insertion
- Export
- On-Chip Clocking (OCC)
- DFTMAX
- Advanced Topics

**Course 4: DC: SystemVerilog for RTL Design**
- Introduction
- SystemVerilog Features
- Implementing User Logic Intent
- Combinational Logic/Latches
- Meaning of full/parallel
- Registers
- State Machine
- Wildcard & Tri-state logic
- Pack/Unpack Array & Struct/Union
- Interface & Package
- Achieving High QoR-Coding

### Legend
- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
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DSO.ai Learning Path

Course 1

DSO: Foundation

Introduction
Cold Start
Warm Start

Legend

Self-paced Learning
Instructor-Led Training
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Duration in Days
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ESP Learning Path

Course 1

ESP: Jumpstart

Legend

Self-paced Learning
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Downloadable Lab
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Duration in Days
Badge

Introduction
Symbolic Simulations
Functional Accuracy
PIV Introduction
# Fusion Compiler Learning Path

## Course 1: FC: Jumpstart
- Introduction
- Design Setup and Reading RTL Design
- NDMs/CLIBS
- Floorplan and UPF data
- Compile Flow
- Timing Setup and CCD
- Power Optimization
- Top Level Synthesis
- Design Implementation

## Course 2: FC: Design Creation & Synthesis
- Introduction & GUI
- Reading RTL
- Objects, Attributes, Application Options
- Compile Flows and Setup
- NDM Cell Libraries
- Loading UPF and Floorplan
- Timing Setup & OCV
- CCD Optimization
- Power Optimization
- Additional Compile Settings and Techniques
- Hierarchical Synthesis

## Course 3: FC: Design Implementation
- Floorplanning
- Setting up CTS
- Running CTS (CCD+classic flow)
- Routing
- Routing DRC
- Via Ladder
- Post-route Optimization
- Signoff

## Course 4: FC: DFT Insertion
- Introduction
- Scan Testing and Flows
- Test Protocol
- DFT Design Rule Checks
- DFT DRC GUI Debug
- DRC Fixing
- Top-Down Scan Insertion
- Advanced Scan Insertion
- Bottom-up Scan Insertion
- Export
- On-Chip Clocking (OCC)
- DFTMAX
- Advanced Topics

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**Legend**
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FC/ICC II Hierarchical Design Planning Learning Path

Course 1

**DP: SOC Design Planning**

- Initial Design Planning
- IO Planning
- From Commit to Abstract Creation
- VA and Block Shaping
- Macro Placement
- PG PPNS
- Pin Placement
- Timing and Budgeting
- Integration/Assembly
- Integration/Assembly

**Legend**

- Self-paced Learning
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Fusion Platform Methodology Learning Path

Course 1

FPM: Jumpstart

- Introduction & Overview
- Organization & Structure
- Lab Example
- Installation & Setup
- FCRM for FPM Users
- FAQ – Common Topics

Legend

Self-paced Learning
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IC Compiler II Learning Path

Course 1
- Introduction
- Design/Timing Setup
- NDMs/CLIBS
- Floorplan
- Placement & Optimization
- Clock Tree Synthesis
- Routing
- Top Level Synthesis
- Design Implementation

Course 2
- GUI Usage (lab)
- Objects, Attributes, Application Options
- Floorplanning
- Placement
- NDM Cell Libraries
- Design Setup
- Timing Setup
- Setting up CTS
- Running CTS (CCD+classic flow)
- Routing
- Via Ladder
- Post-route Optimization
- Top Level Implementation

Legend
- Self-paced Learning
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Synopsys Confidential Information
IC Validator Learning Path

Course 1
ICV: User (DRC & LVS)

- Setup ICV and run DRC/LVS testcase
- DRC Error Classification
- Execute DRC testcase with select commands
- LVL
- Edtext options
- Generate ICV formatted netlist
- Generate equivalence options
- Debug LVS errors
- Using Short finder
- Using VUE & ICVWB with ICV

Course 2
ICV: Runset

- Overview
- Language introduction
- Command API
- Writing a simple "flat" rule runset
- Running a simple IC Validator runset
- Advanced programming concepts
- IC Validator API header files
- Runset coding practices
- Layout device extraction
- Benefits of new language
- Runset structure
- Anatomy of device extraction functions
- Property calculation
- User-defined property functions

Legend
Self-paced Learning
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### Language Learning Path

#### Course 1: Introduction to SVA
- Introduction
- Types of Assertions
- Action Blocks
- Disabling/Combining/Embedding Assertions
- Controlling Assertions
- Sequences and Sequence Repetition
- Sequences Operators
- Synthesis Assertion Coverage
- Assertion Libraries

#### Course 2: System Verilog Assertion
- Basic System Verilog Features
- Implementing User Logic Intent (combinatorial logic & latch)
- Implementing User Logic Intent (meaning of full and parallel)
- Implementing User Logic Intent (implementing registers)
- Implementing User Logic Intent (implementing state machines)
- Implementing User Logic Intent (wildcard and tri-state logic)
- Advanced System Verilog Features (packed or unpacked array and struct)
- Advanced System Verilog Features (System Verilog interface)
- Advanced System Verilog Features (System Verilog package)

#### Course 3: System Verilog for RTL Design
- Achieving High QoR Through Coding
- The Device Under Test
- System Verilog Verification Environment
- System Verilog Testbench Language Basics - 1
- System Verilog Testbench Language Basics - 2
- Managing Concurrency in System Verilog
- Object-Oriented Programming: Encapsulation
- Object-Oriented Programming: Randomization
- Voltage Dependent Rule Check
- Object-Oriented Programming: Inheritance
- Inter-Thread Communications
- Functional Coverage
- System Verilog UVM preview

#### Course 4: System Verilog Testbench
- Self-paced Learning
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- Duration in Days
- Badge

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Legend:
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Language Learning Path (Page 2)

Course 5

L: System Verilog Verification using UVM

- System Verilog OOP
- Inheritance Review
- UVM Structural Overview
- Modeling Stimulus (UVM Transactions)
- Creating Stimulus Sequences (UVM Sequence)
- Component Configuration and Factory
- TLM Communications
- Scoreboard & Coverage
- UVM Callback
- Advance Sequence/Sequencer
- Phasing and Objections
- Register Layer Abstraction (RAL)
- Summary

Legend

- Self-paced Learning
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PrimeLib Learning Path

Course 1

Legend
- Self-paced Learning
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- Duration in Days
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PL: Foundation

Tool Introduction
Global Setting to start characterization
Cell Level Setting to Configure Arcs
Different Characterization flow
Creating multiple Connect Database
Debugging and Troubleshooting
Complex Cell Characterization
Timing Characterization
Constraint Timing Characterization
Power Characterization

1
Timing Characterization
Constraint Timing Characterization
Power Characterization

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## PrimePower Learning Path

### Course 1

<table>
<thead>
<tr>
<th>PP: Jumpstart</th>
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</thead>
<tbody>
<tr>
<td>Power Analysis Input</td>
</tr>
<tr>
<td>Power Components</td>
</tr>
<tr>
<td>Leakage Power</td>
</tr>
<tr>
<td>Internal Power</td>
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<tr>
<td>Switching Power</td>
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<tr>
<td>Inputs &amp; Outputs of Power Analysis</td>
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<tr>
<td>Simulation Activity Files</td>
</tr>
<tr>
<td>Flow &amp; Report</td>
</tr>
</tbody>
</table>

### Course 2

<table>
<thead>
<tr>
<th>PP: Foundation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introduction</td>
</tr>
<tr>
<td>Power Analysis</td>
</tr>
<tr>
<td>Power Components</td>
</tr>
<tr>
<td>Leakage Power</td>
</tr>
<tr>
<td>Internal Power</td>
</tr>
<tr>
<td>Switching Power</td>
</tr>
<tr>
<td>Leakage &amp; Internal Power Data</td>
</tr>
<tr>
<td>Input &amp; Outputs of Power Analysis</td>
</tr>
<tr>
<td>PrimePower Analysis Modes</td>
</tr>
<tr>
<td>Simulation Activity Files</td>
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<tr>
<td>RTL Activity Flow</td>
</tr>
<tr>
<td>Gate-Level Activity Flow</td>
</tr>
<tr>
<td>PrimePower Analysis Accuracy</td>
</tr>
<tr>
<td>PrimePower Standalone – ASCII Flow</td>
</tr>
</tbody>
</table>

### PrimePower – Session Based Flow

- Check & Report Power
- Report Switching Activity
- Summary

### Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge
## PrimeSim Learning Path

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<tr>
<td>PS: Jumpstart</td>
<td>PS: Foundation</td>
<td>PS: Advance</td>
<td>PS: Advance</td>
</tr>
<tr>
<td>PrimeSim Static CCK Introduction</td>
<td>PrimeSim XA Introduction</td>
<td>CCK Advanced ERC and ESD Checks</td>
<td>Interactive Mode</td>
</tr>
<tr>
<td>PrimeSim CCK Built-In Checks</td>
<td>PrimeSim XA Nelist format Support</td>
<td>CCK Propagation Engine – XPL and Analog Propagation</td>
<td>Distributed Processing</td>
</tr>
<tr>
<td>PrimeSim CCK Interactive Debugging Commands</td>
<td>PrimeSim XA Analyses support</td>
<td>CCK Custom Programmable Checks</td>
<td>Monte-Carlo (MC)</td>
</tr>
<tr>
<td>PrimeSim CCK False Error Pruning</td>
<td>Command/Option Usage &amp; Precedence Rules</td>
<td>Custom Check Assertion</td>
<td>MOSRA</td>
</tr>
<tr>
<td>Custom Compiler – PrimeSim CCK : Setup and run</td>
<td>PrimeSim XA Post-Layout Simulation</td>
<td>GUI : Cross-Probe, Filtering, Waiver, Grouping, export</td>
<td>Aging and Self-Heating</td>
</tr>
<tr>
<td></td>
<td>PrimeSim XA Command Line Usage</td>
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<td>PrimeSim XA Log File Details</td>
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<td>Accuracy and Speed Trade-off</td>
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<td>Back-Annotation &amp; XBA</td>
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<td>Probing in PrimeSim XA</td>
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<td>PrimeSim XA .ALTER Usage</td>
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<td>PrimeSim XA .DATA Usage</td>
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</tbody>
</table>

### Legend
- **Self-paced Learning**
- **Instructor-Led Training**
- **Downloadable Lab**
- **Cloud-based Lab**
- **Duration in Days**
- **Badge**
# PrimeTime Learning Path

## Course 1: PT: Jumpstart
- **Overview**
- PrimeTime Implementation Flow
- PrimeTime Inputs & Outputs
- Timing Analysis Flow
- Load Design & Check
- Load Library & Check
- Read Parasitic & Check
- Source Constraints & Check
- Constraints Completeness
- Coverage Analysis
- Report
- Saving & Exit

## Course 2: PT: Foundation
- Introduction to STA in PrimeTime
- STA Concepts and Flow in PrimeTime
- Methodology: Qualifying Constraints
- Methodology: Generating Reports
- Constraining Multiple Clocks
- Additional Checks and Constraints
- Correlation: POCV and AWP Analysis
- Signoff: Path Based Analysis (PBA)
- Signal Integrity: Crosstalk Delay Analysis
- Signal Integrity: Crosstalk Noise Analysis
- Timing Closure: ECO/What If Analysis
- Large Data: DMSA and HyperScale Analysis

## Course 3: PT: HyperScale
- Introduction HyperScale
- Flat Context Flow
- Bottom Up Flow
- Generating HyperScale Block Models
- Constraint Consistency
- Clock Mapping
- HyperScale Top-Down Flow
- HyperScale-Driven ECO
- Summary

## Course 4: PT: Scalable STA
- Hierarchical Methodologies
- HyperScale
- HyperScale Hybrid Flow
- Distributed & Scenario Analysis
- HyperGrid
- DMSA
- DVFA/SMVA
- PBA Technologies
- Best Practices

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### Legend
- Self-paced Learning
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- Badge
Reference Methodology Learning Path

Course 1

RM: Jumpstart

Legend

Self-paced Learning
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Downloadable Lab
Cloud-based Lab
Duration in Days
Badge

Introduction & Overview
Organization & Structure
Running RM
Demo
RTL Architect Learning Path

### Course 1: RTLA: Jumpstart
- Introduction & Overview
- RTL Architect Key Features
- Predictive Engine
- Unified GUI
- Physical Floorplanning
- Power Analysis
- Logic Restructuring
- Constraint Management
- Flows
- `rtl_opt` Mega Command
- Block-Level Flow/Breakpoints
- Hierarchical Flow/Breakpoints

### Course 2: RTLA: Using RTL Restructuring
- RTL Restructuring
- Group
- Ungroup
- Reparent
- Restructured RTL, SDC, UPF, SAIF Generation
- Reparenting and Writing RTL
- Demo

### Legend
- Self-paced Learning
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- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge
StarRC Learning Path

Course 1

SRC: Jumpstart

- Interconnect
- Coupling Capacitance
- Classes of Extractors
- Input for Parasitic Extraction
- StarRC Flow
- SMC Flow
- ITF File

Course 2

SRC: Foundation

- Extraction Fundamentals
- Gate level Extraction
- Transistor Level Extraction
- Selective Netlist
- Field Solver
- Process Modelling
- Metal Fills

Legend

- Self-paced Learning
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- Badge
Saberr RD Learning Path

Course 1

SRC: Foundation
Training Series

Timing Domain Analysis
Schematic Capture & Parts Library
Operating Points & Small Signal Frequency Analysis
Test Automation
Design Optimization
Introduction to Modeling
Import SPICE Models
Modeling with Table Look-Up
Modeling with StateAMS
Robust Design & Sensitivity Analysis
Monte Carlo & Pareto
Worst-Case Analysis
Fault Analysis
Stress Analysis

Legend

Self-paced Learning
Instructor-Led Training
Downloadable Lab
Cloud-based Lab
Duration in Days
Badge
Synplify: Learning Path

Course 1

S: Foundation

- Introduction to Synplify Elite Flow
- Creating and Running Synplify Project
- View Log File
- HDL Analyst
- Handling High Reliability Designs
- Implementing Fault Tolerant FSMs
- ECC RAM Inferring
- Importing Quartus IP in Synplify Projects
- Debugging with SpyGlass
- Debugging with VCS
- Identify Instrumentor and Debugger

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge

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TestMAX Advisor Learning Path

Course 1

TMA: Jumpstart

- Early Testability Goals and Reports
- Debug using the GUI
- Transition Delay Checks
- Random Resistant Fault Analysis and Test Points
- Post stitch DRC Checks
- Connectivity Checks
- Flow With TestMAX Manager

Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge
# TestMAX Access Learning Path

## Course 1

**TMA: Jumpstart**

- TestMAX Access structure
- IEEE 1687 interface to drive internal instruments through TDR
- SIBs
- Define Ring configuration
- Definition of Server and Subserver
- AIT
- PDL Pattern Porting
- PDL data packetization
- Validation of AIT

## Course 2

**TMA: ATPG & Diagnosis**

- Manufacturing Test and ATPG
- Building ATPG Models
- Running DRC
- Fault Models and Managing Faults
- Controlling ATPG
- Post ATPG Analysis
- Pattern Validation
- At-Speed Testing and Constraints
- Transition Delay Testing
- On-Chip Clocking and Compression
- Diagnosis

### Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge

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TestMAX FuSa Learning Path

Course 1

TMF: Jumpstart

Functional Safety for Automotive Designs

TestMAX FuSa: Introduction

TestMAX FuSa: Static FuSa Analysis

Running TestMAX FuSa: Requirement & Constraints

Functional Safety reporting in TestMAX FuSa

Legend

Self-paced Learning

Instructor-Led Training

Downloadable Lab

Cloud-based Lab

Duration in Days

Badge
# TestMAX SMS Learning Path

## Course 1
- TM-SMS: Architecture
  - Introduction
  - SMS Wrapper
  - SMS Processor
  - MMB Processor
  - SMS Server
  - Conclusion

## Course 2
- TM-SMS: Flow
  - SMS Hierarchical Flow & User Interface
  - File Structure
  - BIST Customizations
  - Validation Flow
  - Diagnosis Flow
  - Lab

## Legend
- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge
# TestMAX XLBIST Learning Path

## Course 1

### TMXB: Jumpstart

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<th>LogicBIST basics</th>
<th>Troubleshooting and Debug hints</th>
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<tbody>
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<td>XLBIST architecture</td>
<td>Intro to AIT</td>
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<tr>
<td>XLBIST and SEQ modes of operation</td>
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<tr>
<td>IEEE 1500 I/F and internal resources</td>
<td></td>
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<tr>
<td>XLBIST patterns and interval definition</td>
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<tr>
<td>Random Resistant Fault analysis and Test Point insertion</td>
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<tr>
<td>X propagation analysis and fixing</td>
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<tr>
<td>OCC and Clock Weights</td>
<td></td>
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<tr>
<td>Reset Controller and Reset Weights</td>
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<tr>
<td>Programmable SE Timing Margin</td>
<td></td>
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<tr>
<td>Remap XLBIST Patterns for Debug and Diagnosis</td>
<td></td>
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<tr>
<td>Validation of XLBIST patterns</td>
<td></td>
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<tr>
<td>Porting of XLBIST patterns</td>
<td></td>
</tr>
<tr>
<td>Simulation steps for validation</td>
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</tr>
</tbody>
</table>

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### Legend

- **Self-paced Learning**
- **Instructor-Led Training**
- **Downloadable Lab**
- **Cloud-based Lab**
- **Duration in Days**
- **Badge**
Zebu Learning Path

Course 1
- Zebu: Foundation
  - Introduction to Emulation
  - ZeBu overview (HW and SW)
  - ZeBu Ecosystem
  - ZeBu Compile
  - ZeBu Runtime
  - Tuning ZeBu for High Performance / TAT / Capacity
  - Gate Level emulation

Course 2
- Zebu: Advance
  - Transactors – Guide to integration + List
  - Low Power emulation
  - Virtual Host and Devices
  - ZeBu Debug
  - Hybrid Emulation
  - ZeBu Empower – SW based power analysis
  - Real world interfaces with speed adaptors

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