SYNOPSYS®

Signoff SIG • November 2, 2023

AGENDA

TIME	Thursday, November 2, 2023		TIME
11:30 – 12:15 PM	**REGISTRATION CHECK-IN & LUNCH**		11:30 – 12:15 PM
12:15 – 12:50 PM	**WELCOME ADDRESS and INTRODUCTION** **Synopsys Signoff Vision** **Jacob Avidan, Senior Vice President, Engineering, Synopsys** ***Room: Otto/Davis***		12:15 – 12:50 PM
	Signoff Track ***Room: Otto/Davis***	**Physical Signoff & ESD Track** ***Room: Bohlin***	
12:55 – 1:20 PM	Distributed STA and ECO for Next Generation Hyperscaler Designs *– Sarvesh Ganesan - Microsoft*	Performance Improvements at Full Chip Level using IC Validator Elastic on Intel XEON Design *– Matt Nichelson - Intel*	12:55 – 1:15 PM
1:20 – 1:45 PM	Synopsys PrimePower + Power Replay Flow *– Vishnu Pothireddy - Cisco Systems*	Unlocking the Potential: Advanced StarRC Extraction Methodologies for Accurate Custom/RF Design Closure *– Krishnakumar Sundaresan - Synopsys*	1:15 – 1:45 PM
1:45 – 2:10 PM	Leveraging PrimeShield Voltage Slack Analysis To Build Vmin Robust Designs and Explore the Lowest Possible Vmin Reduction *– Muniswara (Munish) Raja - Intel*	Improving Design ESD Robustness with Full Chip CDM Simulation *– Srinivas Velivala - Synopsys*	1:45 – 2:10 PM
2:10 – 2:25 PM	**BREAK**		2:10 – 2:25 PM
2:25 – 2:50 PM	Hyperscale Based Large Subsystem Timing Closure using Synopsys Tweaker ECO *– Ramesh Murugesan - NVIDIA*	Improving PMIC & Power Transistor Design Efficiency & Reliability in Advanced Technologies *– Philipp Lindorfer - Synopsys*	2:25 – 2:50 PM
2:50 – 3:15 PM	IR Aware STA for Advanced Process Nodes *– Srinivas (Sri) Chilukuri - Qualcomm*	Synopsys IC Validator Productivity Features for Faster Signoff *– Ramulu Undevalli - NVIDIA*	2:50 – 3:10 PM
3:15 – 3:30 PM	Migrating to Synopsys PrimeClosure	*Synopsys IC Validator Demo*	3:10 – 3:30 PM
3:30 – 4:30 PM	**NETWORKING RECEPTION** ***Room: Bosch***		3:30 – 4:30 PM