Verification Symposium – October 10th – Daniel Hotel Herzelia

Time	Session Title	Presenter	Notes
08:30-09:30	**Registration + Breakfast**		
09:30-10:30	**System Verification in the World of Software-Defined Products: The Next Frontier**	Ravi Subramanian, GM Systems Design Group	General session (SW+HW)
10:30-11:15	**Synopsys Solutions for Energy Efficient Design**	Asi Sapir	General session (SW+HW)
11:15-11:30	AM Break		
11:30-12:15	**End-to-End Protocol Solutions**	Antonio Costa	General session (SW+HW)
12:15-13:00	**Cloud-powered EDA by the Minute: Maximizing productivity with EDA on AWS**	AWS	General session (SW+HW)
13:00-14:00	**Lunch and split into SW and HW Sessions (See below the SW and HW agendas)**		
17:00-17:30	*Wrap up/Prize Draw*		

14:00-14:45	**Why wait for Gate Level Simulation to verify your SDC?**	Arik Rachevsky Avi Levi	SW Session
14:45-15:30	**From good to great, how Formal sign-off can improve design quality and accelerate verification closure**	Tushar Parikh	SW Session
15:30-15:45	PM Break		
15:45-16:15	**How AI and other advanced technologies can boost your verification schedule**	Shlomo Levy	SW Session
16:15-17:00	**Hyperconvergence – Static Signoff across RTL2Gate Flow**	Deepak Ahuja	SW Session

14:00-14:45	**Hardware-assisted Verification – a use case journey**	Ritesh Goel	HW Session
14:45-15:30	**Software development leveraging Virtual Host**	Ritesh Goel	HW Session
15:30-15:45	PM Break		
15:45-16:15	**System-Level Monitoring and Debug Methodologies for HAV platforms**	Ritesh Goel	HW Session
16:15-17:00	**Advanced Prototyping with HAPS**	Antonio Costa	HW Session