Technology Symposium 2023 - UK

8:30 - 9:30	**Registration and Breakfast**		
9:30 - 10:30	**Welcome and Keynote** **Building Tomorrow's Chips with AI - Thomas Andersen , VP Synopsys**		
10:30 - 11:15	**Fusion Power – Synopsys Energy Efficiency Solution from Architecture to Signoff - Thomas Ryan**		
11:15 - 11:30	**BREAK**		
11:30 - 12:15	***Implementation and Sign off*** ***Moderator:***	***Functional Verification - SW & HW*** ***Moderator:***	***IP:*** ***Moderator***
	RTL Architect Design Platform for convergent design flow - Andrew Saunders - Synopsys	VC Formal™, New Applications for Security and Low Power – Sai Karthik M. - Synopsys	Optimize Your Own RISC-V Architecture, Using Application-Specific Processor Design Tools - Falco Munche - Synopsys
			AMS: ***Moderator***
12:15 - 13:30	**LUNCH BREAK**		
13:30 - 14:15	Design Planning: New Technologies and Trends - Jason Jackson - Synopsys 3DIC Compiler: The Way to Multi-Die Systems	Accelerating Key Use cases with Hardware Assisted Verification - Luca Rastello - Synopsys	Accelerating analog and mixed-signal simulation through PrimeSim Continuum - Andrew Milne - Synopsys
14:15 - 15:00	Advanced node extraction and Physical Verification - David DeMarcos - Synopsys	VC SpyGlass™ New Technologies: CDC Static Aware Synthesis, Synchronous Path Glitch Verification, Formal CDC Using VC Formal™ Engine, Smart Netlist CDC - Bhavesh Patel - Synopsys	Analog Design Retargeting Vision and Case Study - Damian Roberts - Synopsys
			FuSa: ***Moderator***
15:00 - 15:15	**BREAK**		
15:15 - 16:00	STA trends & Comprehensive SDC Timing Constraints Generation, Verification and Management Using Timing Constraints Manager - Simon Bloyce , Bhavesh Patel - Synopsys	The Era of Autonmous Verification - Piyush Sukhija - Synopsys	Synopsys Functional Safety technologies update for E2E secure design - Bob Fairey - Synopsys
16:00 - 16:45	Golden Sign off ECO - Simon Bloyce - Synopsys	Verdi® Debug for Productivity & VCS Technology Updates - Pushkar Kumar - Synopsys	
16:45 - 18:00	**SOCIAL EVENT**		