SYNOPSYS®

Verification Day 2020

A Special Interest Group Virtual Event

Agenda At-A-Glance

October 8, 2020			
9:00am – 3:00pm PDT	**Demo Lounge**		
9:00am – 9:30am PDT	**Keynote Panel** How Verification Technologies Have Evolved to Support Chip Complexity *– Synopsys*		
	Formal Verification	Static Verification	Low Power Technology
9:30am – 10:10am PDT	Verification Avengers—How Formal Super Heroes Save the Day *– Synopsys*	CDC/RDC Strategy and Signoff Methodology *– Analog Devices, Inc.*	Low Power Static Checking—New Challenges and Solutions *– Qualcomm*
10:10am – 10:50am PDT	Formally Signing-off Floating Point Datapath *– Intel*	Constraints Driven Clock Domain Crossing Signoff *– Facebook*	Power Model Framework with VCS, UPF, PrimePower and VCS NLP *– Microsoft*
10:50am – 11:30am PDT	From Apps to Signoff: Climbing the Formal Deployment Pyramid *– Qualcomm (3a)* Fastest Functional Coverage Development and Closure with Formal *– Qualcomm (3b)*	Asynchronous Reset Logic Verification *– Xilinx*	Isolation Checks During a Pandemic *– Intel*
11:30am – 11:40am PDT	**10-Minute Break**		
11:40am – 12:10pm PDT	Ingredients for Creating A Success Story in RTL to RTL Equivalence Verification *– Samsung Austin Research Center (SARC)*	Enabling Customer Success Through Robust CDC Methodology *– Synopsys*	Perform Multi-Voltage Checks Faster with Low Power Signoff *– Synopsys*
12:10pm – 12:40pm PDT	Eliminating Block Level Simulations with Full Formal Signoff *– Synopsys*	Advanced Technologies in Static Verification *– Synopsys*	Achieving Successful Low Power Verification on A Tight Schedule *– Facebook*

Presentation Abstracts

Sean Safarpour,
Group Director of
Application Engineering,
Synopsys

Verification Avengers—How Formal Super Heroes Save the Day

Presentation Abstract

In today's uncertain world, the ever-growing, complex and time-sensitive nature of the verification problem is akin to a super villain. With every design cycle and every iteration, the problem gets bigger and harder to complete/defeat. The future looks pretty grim as millions/billions of simulation/emulation cycles and armies of DV engineers struggle to catch all the bugs while deadline slips loom overhead.

Fortunately, there are super heroes masquerading as engineers armed with the best and latest formal verification tools and methodologies that can take on the verification super villain. The key is to attack from multiple angles. 'Formal Flash' for example uses speed to quickly deploy formal Apps to find bugs faster and more efficiently than others. 'Captain Signoff' takes on the really tricky blocks and performs exhaustive formal verification with his assurance that no bugs will be missed. Finally, 'Stretch the Bug-Hunter' uses the power for formal verification to go after corner-case bugs that no other hero can find. And that is how the Formal Super Heroes Save the Day.

Lijun Li,
Lead Formal Verification
Engineer,
Intel

Formally Signing-off Floating Point Datapath

Presentation Abstract

Floating point datapath is known to be one of the most challenging verification problems to solve. There is usually no UVM simulation testbench built for the mathematical components and functional coverage model is hard to implement due to many corner cases, thus this is a sweet spot for formal verification. In this presentation, Lijun Li will describe C2RTL equivalence check to prove math intensive floating point datapath functions and share his success story of DPV (Datapath Verification) for the GPU design.

Ipshita Tripathi,
Formal Verification Lead,
Qualcomm

3a. From Apps to Signoff: Climbing the Formal Deployment Pyramid

Presentation Abstract

Formal deployment is often a challenge faced in many organizations. Formal verification scope is wide and there are number of use-cases where users can focus to get verification benefits. As most people are aware, there are two ends of the spectrum where formal verification provides immediate value. One of the areas is the use of formal apps to solve a particular verification problem such as connectivity or register verification or bus certification. These are often easier to use from a user perspective without any expertise building, and thus easily adopted by wide audiences. Its advantages include a significant left shift using these apps/AIPs in the entire verification effort.

The other end of the spectrum involves the improvement in quality by finding more complex issues that can only be uncovered due to the exhaustiveness that formal brings to the verification effort. This involves expertise building in the team to see maximum ROI from the verification.

The final aim as we engage in this is to be able to replace some areas of the verification completely with formal verification rather than it being an add-on to the existing effort or to be able to formally signoff on some areas of the design. The path to formal signoff is not straightforward and is only possible deploying formal bug hunting in many designs to find interesting bugs. In the process of this, the team also builds expertise and can gradually get involved in the more complex problems related to signoff and can move higher in the pyramid.

In this talk, Ipshita Tripathi will talk about some of her experiences while traversing this pyramid- the areas where she has seen good returns and some of the newer areas in which she continues to engage as well as how she is ramping up more of the team to be conversant in formal verification methods and enabling them to climb the pyramid.

Presentation Abstracts

Luv Sampat,
Engineer,
Qualcomm

Matt Cummings,
Sr. Staff Engineer,
Qualcomm

3b. Fastest Functional Coverage Development and Closure with Formal

Presentation Abstract

Closing the last 10% of functional coverage often requires multiple calendar weeks and engineering man months of effort. One of the more difficult tasks can be identifying bad uncovered points and crosses as this can be equivalent to proving a negative. In this discussion, Luv Singh will present a formal solution that can identify in hours what used to take multiple days per unhit point—Unreachability Analysis (UNR)—which like the synthesis tools analyzes the RTL cone of logic against the coverage model to identify if "coverage holes" are reachable, offering significantly faster feedback on uncovered bins. Further, for heavily parameterized designs, he will provide a template expansion approach to expand directives embedded in a SystemVerilog file to generate cover groups, points and bins based on design parameters.

Together, they result in a leaner coverage model tuned to the design and void of bad coverage that leads to higher quality coverage reports and increased efficiency.

Arun Singh,
Formal Verification Engineer,
Samsung Austin Research Center (SARC)

Ingredients for Creating A Success Story in RTL to RTL Equivalence Verification

Presentation Abstract

Retiming is used to meet design performance, power and area requirements and it should not impact the core functionality of the circuit. It is very critical to confirm that these changes do not alter the functionality of the design. Designers and verification engineers have multiple ways to approach this verification problem and in recent times formal verification has proven to be the most productive method. In this presentation, Arun Singh will discuss various formal Apps that can be leveraged to address this problem.

Iain Singleton,
Staff Applications Engineer,
Synopsys

Paul Stravers,
Principal R&D Engineer,
Synopsys

Eliminating Block Level Simulations with Full Formal Signoff

Presentation Abstract

In this presentation, Iain Singleton from the Synopsys VC Formal team and Paul Stravers from the ARC HS design team discuss a case study project, taking a brand-new block and verifying it entirely with formal. They will focus on the steps from planning through signoff, formal's ability to find interesting issues quickly, and what it was like for a design engineer playing with formal debug for the first time. In the end, they will demonstrate how taking a chance by dropping simulation at the block level can provide great results quickly and how design engineers adapt to the process.

Presentation Abstracts

Alberto Carbajo,
IC Digital Design Engineer,
Analog Devices, Inc.

CDC/RDC Strategy and Signoff Methodology

Presentation Abstract

This presentation will describe a strategy to minimize CDC and RDC issues in silicon.
The presentation will start with a brief recap of CDC and RDC issues, followed by a list of recommendations and good practices to avoid metastability issues. The second part of the presentation will focus on the signoff methodology along with some 'gotchas' found in the past when analyzing different designs.

Ivan Svestka,
Digital Design Engineer,
Facebook

Constraints Driven Clock Domain Crossing Signoff

Presentation Abstract

The goal of this presentation is to provide an overview of the clock domain crossing (CDC) problem and how it impacts signoff. It will discuss issues observed in the CDC flow and how to best address them. This includes the discussion of constraints versus waivers and using dynamic verification to drive higher quality CDC.

Mark Kelley,
Sr. Staff Engineer,
Xilinx

Asynchronous Reset Logic Verification

Presentation Abstract

Combinational logic finds its way onto the asynchronous reset path through test, ECO or designed in intentionally. These paths must be glitch free. The standard RTL flow is not able to detect if the reset path is glitch free in simulation or formal verification. Many glitch sources are the result of poor physical implementation. This presentation will discuss a process to prevent glitches in the first place. We will then show how seemingly safe logic can end up with a glitch on the reset path. There are different types of glitches that will be reviewed. The presentation concludes with how to handle existing glitches in the design.

Luis Laranjeira,
Director, R&D,
Synopsys

Enabling Customer Success Through Robust CDC Methodology

Presentation Abstract

Being a leading silicon IP provider comes with huge responsibility for Synopsys. System-on-Chip integrators rely on proven silicon IP as building blocks to assemble ever more complex solutions, with multiple industry protocols processed in parallel via dedicated multi-clock subsystems, where IP quality becomes critical in the race for chip production. This presentation shows how Synopsys addresses the challenge of Clock Domain Crossing verification of its silicon IP, which is essential for enabling its successful integration into System-on-Chips.

Rajarshi Mukherjee,
Group Director, R&D,
Synopsys

Advanced Technologies in Static Verification

Presentation Abstract

In this talk Rajarshi Mukherjee will present advanced technologies in two broad areas. The first area is noise reduction and root-cause analysis. Large violation count is often a challenge in static verification tools. Sometimes multiple violations may point to different facets of a given problem. These can make it challenging to figure out the exact nature of the problem and how one should fix it. Synopsys has developed Machine Learning-based technologies to significantly improve designer debug productivity. He will show customer examples where this technology has accurately found root-causes for violations and how customers have been able to fix design issues much faster.
The second area is improvement of a certain class of Lint checks using Formal Verification. In this talk, Rajarshi will also introduce a class of problems that are amenable to improvements using formal verification and explain how formal verification improves the quality of results of related Lint checks.

Presentation Abstracts

Sayandeep Nag,
Sr. Staff Engineer Manager,
Qualcomm

Low Power Static Checking—New Challenges and Solutions

Presentation Abstract

Low Power static checks are required at multiple stages of the design cycle and can be used to validate the sanity of the design with respect isolation and retention among other low power infrastructure elements. They ensure that the proper control signals are available in the required hierarchies, can be used to sanitize the power intent and the library components required for power-aware synthesis and verification, and, most importantly, to signoff the entire design for power structural checks before tape out. An engineer owning and signing the low power static checks is expected to have complete understanding of the system-level behavior of the design under validation so that it can be validated in the right set of scenarios. He is expected to provide the correct requirements for the necessary design modifications and thus ensure structural and functional sanity.
With the increased complexity of design and the need to save power by having multiple power domains and DCVS modes, it has become critical to have the right set of static low power methodology in place to avoid scenarios which can cause silicon to be dead on arrival. At Qualcomm, over a period of execution of multiple SoC designs, we have come across multiple challenges which required the implementation of innovative solutions but also methodology updates. This talk will capture some of those challenges while designing SoCs up until the final tape out signoff.

Anand Iyer,
Principal Engineer,
Microsoft

Power Model Framework with VCS, UPF, PrimePower and VCS NLP

Presentation Abstract

Traditional power estimation is giving way to design-level power models which are more versatile. They can provide power estimates in varying environments and use cases. Even though the trend is new, power models are not uncommon to designers as they have modeled power of standard cells and SRAMs using similar models; but, as one goes to higher-level abstracts, the task can become quite hard. In this talk we are going to discuss a framework to describe power models. The framework uses Synopsys' tools such as VCS, VCS NLP and PrimePower. We will be showing some examples to illustrate this framework.

Will Crocco,
Corporate Chair for
Multi-voltage Design
Methodology,
Intel

Isolation Checks During a Pandemic

Presentation Abstract

Typically, design teams use Static Multi-Voltage Verification (SMVV) to check the isolation strategies present in UPF and their implementation netlist as part of electrical and functional signoff. Verifying the set of isolation enable signals and their relation to the corresponding supply of the signal being isolated has been historically difficult. In this presentation, we will demonstrate the use and value of a new feature in SMVV, namely Low Power Signal Supply Constraint, to statically verify the isolation enables against the related supply of the signal being isolated.

Presentation Abstracts

Godwin Maben,
Synopsys Scientist,
Synopsys

Perform Multi-Voltage Checks Faster with Low Power Signoff

Presentation Abstract

The typical low power signoff process involves extracting data from place and route (P&R) tools like Synopsys IC Compiler™ II and Fusion Compiler and analyzing the design using Synopsys VC LP to identify electrical violations. The integration of VC LP within IC Compiler II enables P&R engineers to verify the signoff checks before passing the data to VC LP, thus greatly reducing the turnaround time and enabling faster signoff closure.

In this session we will highlight the benefits of tight integration between P&R and low power signoff tools including:

- The ECO process of fixing multi-voltage violations based on signoff checker in IC Compiler II P&R
- How to apply global project-based signoff waivers at P&R stage
- How to improve ECO process efficiency and reduce overall turnaround time

Yuan Zong,
Design Verification Engineer,
Facebook

Achieving Successful Low Power Verification on A Tight Schedule

Presentation Abstract

Low power verification is playing a crucial role in the overall chip validation as any missed bugs could be design-kill. Low power verification not only depends on the RTL design and testbench, but also on the UPF, liberty libraries and power management units (if using a 3rd party IP). Any of those inputs could be that shortest stave in a barrel, causing delays and requiring expensive fixes. A well-defined low power verification methodology along with a cross-functional team collaboration is necessary to overcome that challenge.

In this presentation, we will share how Facebook completed low power verification in multiple IPs with tight schedules and limited resources.

We will review:

- Building a low power friendly testbench
- A common low power testplan and checklist across IPs
- Using VC LP earlier as pipe cleaners
- Using VCS NLP design attribute for quick workaround
- Low power checker and testcase generation